

REVISION RECORD						
REV	TYPE	CHG BY/DATE	CHK BY/DATE	CHK CODE	CHK NO.	REV

UNLESS OTHERWISE SPECIFIED:

DIMENSIONS IN:
MILLIMETRES ☐
INCHES ☒

REFER TO 68P200 FOR DIM INTERPRETATION

THIRD ANGLE PROJECTION ☒



MAXIMUM SURFACE TEXTURE ☒

OVER	TO	TOLERANCE

ANGLES: ☒

XEROX MATERIAL SPEC		RELATED SPECIFICATIONS	
XEROX FINISH SPEC			
APPROVAL SIGNATURES	DATE	REFERENCE CODES	
DRAWN <i>[Signature]</i>			
CHECKED <i>[Signature]</i>			
ENGRS <i>[Signature]</i>			

ITEM	PART NUMBER	DESCRIPTION	QTY
XEROX			
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TITLE: PWB ASSEMBLY, IOP			
DWG NUMBER: 14052450X			
SIZE: SHEET 2 OF 2			

- 1.0 ASSEMBLY MUST MEET ALL THE REQUIREMENTS OF 88P220.
- 2.0 COMPONENT HEIGHT SHALL NOT EXCEED .50 INCH.
- 3.0 UNLESS OTHERWISE SPECIFIED:
CAPACITANCE VALUES ARE IN MICROFARADS.
RESISTANCE VALUES ARE IN OHMS.
RESISTORS ARE 0.25 W.
RESISTANCE TOLERANCES ARE ± 5 PERCENT.
- 4.0 THE PADS FOR THE POSITIVE TERMINALS OF CAPACITORS AND THE CATHODES OF DIODES ARE CIRCLED.
- 5.0 ON THE PWB, A " + " SYMBOL IS MARKED ADJACENT TO THE POSITIVE TERMINAL OF POLARIZED CAPACITORS. THE ARROWHEAD OF THE SYMBOL "  " BETWEEN PADS, POINTS TO THE CATHODE TERMINAL PAD FOR DIODES.
- 6.0 SEMICONDUCTORS ARE TO BE SCREENED ACCORDING TO THE REQUIREMENTS OF 156P11828. IN THE EVENT OF CONFLICT, THE COMPONENT SPECIFICATION TAKES PRECEDENCE.
- 7.0 THE GENERIC PART NAMES LISTED IN THE DESCRIPTION FIELD ARE FOR REFERENCE ONLY. ALL ITEMS MUST BE PURCHASED TO THE REQUIREMENTS OF THE XEROX COMPONENT SPECIFICATION.
- 8.0 HAYWIRES ARE ACCEPTABLE WITHIN THE LIMITS AND REQUIREMENTS OF 082P80232.
- 9.0 MAXIMUM PROTRUSION SOLDER SIDE IS .10 INCH.
-  10.0 ELECTROSTATIC SENSITIVE DEVICE, PROVIDE ADEQUATE PROTECTION FROM ELECTROSTATIC DISCHARGE PER 88P220, SECTION 17.0 (SEE SHEETS 3.1, 3.2 AND 3.3).

PROPRIETARY NOTE ON SHEET 1 APPLIES TO ALL SHEETS

TITLE PWB ASSEMBLY, IOP	DWG. SIZE A4	DWG. NO. 140S2650X	SHEET REV D
		SHEET 2.0 OF	

11.0

SEE SHEET 4.0.

12.0

SEE SHEET 4.0.

13.0

SEE SHEET 4.1.

14.0

TESTING TO BE PERFORMED PER THE APPROPRIATE TEST
SPECIFICATION (SEE SHEET 3.2).

15.0

ALTERNATE PART (SEE SHEET 3.3).

PROPRIETARY NOTE ON SHEET 1 APPLIES TO ALL SHEETS

TITLE

PWB ASSEMBLY, IOP

DWG.
SIZE

A4

DWG.
NO.

140S2650X

SHEET 2.1 OF

SHEET
REV
D

XEROX

REFERENCE DESIGNATION	ITEM	PART NUMBER	DESCRIPTION	QUANTITY REQUIRED PER ASSEMBLY												
				0	1	2	3	4	5	6	7	8	9			
				REV	REV	REV	REV	REV	REV	REV	REV	REV	REV			
				B	A											
	1	140P12114	PWB DETAIL, IOP	1	1											
	2	156P11952	SCHEMATIC, IOP	REF	REF											
	3	003P87082	EXTRACTOR	2	2											
	4	030P87014	STIFFENER, (FRONT)	1	1											
	5	030P83244	STIFFENER, (BACK)	1	1											
	6	091P87222	LABEL, IOP	1	1											
	7	091P87219	LABEL, PWB ASSY	1	1											
	8	713W20725	SOCKET, 24-PIN	4	4											
	9	713W20625	SOCKET, 40-PIN	1	1											
	10	320W13201	RIVET	7	7											
C1,2	11	702W08901	CAP., 10, 25 V	2	2											
C3 THRU 12, 14 THRU 66. 72	12	702W05218	CAP., 0.1, 50 V	64	64											
C13	13	702W02418	CAP., 0.001, 100 V	1	1											
C67,69	14	702W28005	CAP., 22, 35 V	2	2											
C68	15	702W17105	CAP., 68, 15 V	1	1											
CR1,3	16	707W00642	DIODE 1N4003	2	2											
F1,3	17	708W11302	FUSE, 7 AMP	2	2											
F2	18	708W11502	FUSE, 15 AMP	1	1											
J1	19	713W21830	CONN, 18 PIN	1	1											
P11	20	713W15120	CONN, 14 PIN	1	1											
P12	21	713W12220	CONN, 10 PIN	1	1											
P13	22	713W12720	CONN, 40 PIN	1	1											
P14	23	713W10820	CONN, 50 PIN	1	1											
Q1	24	707W01916	TRANSISTOR 2N2905A	1	1											
R1,26,28	25	703W34688	RES, 10 k	3	3											
R2	26	703W35088	RES, 15 k	1	1											
R3,4	27	703W31488	RES, 470	2	2											
R5	28	703W35888	RES, 33 k	1	1											
R6	29	703W29888	RES, 100	1	1											
R7,17,18	30	703W30688	RES, 220	3	3											
R8,11 THRU 16,27,29,30	31	703W32288	RES, 1 k	10	10											
R9	32	703W26687	RES, 4.7, 0.5 W	1	1											
PROPRIETARY NOTE ON SHEET 1 APPLIES TO ALL SHEETS																
TITLE PWB ASSEMBLY, IOP				DWG. SIZE	DWG. NO. 140S2650X										SHEET REV D	
				A4	SHEET 3.0 OF											

REFERENCE DESIGNATION	ITEM	PART NUMBER	DESCRIPTION	QUANTITY REQUIRED PER ASSEMBLY									
				0	1	2	3	4	5	6	7	8	9
				REV	REV	REV	REV	REV	REV	REV	REV	REV	REV
S1	33	710W00002	DIPSWITCH, 2-POLE	1	1								
U1	34	703W01291	R-DIP, 150 x 8	1	1								
U2,17,37,140	35	733W01633	IC, OCT BFR 74S240	4	4								
U3,36,49,90, 128,142	36	733W01698	IC, D-FF 74LS374	6	6								
U4	37	703W30891	R-DIP, 160/260 x 14	1	1								
U5	38	733W00100	IC, DRVR 75114	1	1								
U6,55,87,133	39	733W01705	IC, OR 74LS32	4	4								
U7	40	733W01911	IC, DRVR 75188	1	1								
U8	41	733W00098	IC, RCVR 75189	1	1								
U9,57,107,135	42	733W01704	IC, AND 74LS08	4	4								
U10,25,39,53	43	733W01663	IC, CNTR 74LS393	4	4								
U11,26,40,54	44	733W01674	IC, REG 74LS165	4	4								
U12,47,89,141	45	733W01624	IC, D F-F 74LS273	4	4								
U13	46	537P02280	IC, PROM 93453	1	1								
U14	47	537P02279	IC, PROM 93453	1	1								
U15,137,143	48	733W01640	IC, D F-F 74S374	3	3								
U16	49	733W01916	IC, DATA SEL 74LS153	1	1								
U18	50	733W00378	IC, RCVR 75115	1	1								
U19,24,60,74, 139	51	733W01626	IC, OCT BFR 74LS244	5	5								
U20,41,43,56, 85,86,121,136	52	733W01675	IC, D F-F 74LS74	8	8								
U21	53	537P02283	IC, PROM 93427	1	1								
10.0 U22	54	733W01946	IC, USART 18251A	1	1								
U23,35,48,84, 108,123,127	55	733W01625	IC, OCT BFR 74LS240	7	7								
U27,147	56	733W01643	IC, NOR 74S02	2	2								
U28	57	733W01770	IC, CNTR 74LS163A	1	1								
U29	58	733W01771	IC, D F-F 74S74	1	1								
U30	59	733W01775	IC, MULTIV 74123	1	1								
U31,32,33,34	60	733W01909	IC, CNTR 74LS569	4	4								
U38,120	61	733W01745	IC, MUX 74LS157	2	2								
U42	62	733W00339	IC, HEX INV 7414	1	1								

PROPRIETARY NOTE ON SHEET 1 APPLIES TO ALL SHEETS

TITLE PWB ASSEMBLY, IOP	DWG. SIZE	DWG. NO. 140S2650X	SHEET REV D
	A4	SHEET 3.1 OF	

XEROX

REFERENCE DESIGNATION	ITEM	PART NUMBER	DESCRIPTION	QUANTITY REQUIRED PER ASSEMBLY									
				0	1	2	3	4	5	6	7	8	9
				REV	REV	REV	REV	REV	REV	REV	REV	REV	REV
U44,45,51,134, 144,145,146	63	733W01706	IC, DCDR 74LS138	7	7								
U46,104,105	64	733W01672	IC, HEX INV 74LS04	3	3								
10.0 U50	65	733W02225	IC, TIMER 18253-5	1	1								
U52	66	703W14991	R-DIP, 5.1 k x 15	1	1								
10.0 U58	67	733W02214	IC, FDC FD1797A	1	1								
U59,62,91,109	68	733W01740	IC, XCVR 74LS245	4	4								
10.0 U61	69	733W02232	IC, DMA CONT 18257-5	1	1								
10.0 U63 THRU 70, 76 THRU 83, 94 THRU 101, 111 THRU 118	70	733W01502	IC, RAM 12114	32	32								
U71,72,119	71	733W01671	IC, NAND 74LS00	3	3								
U73	72	703W15691	R-DIP, 10 k x 15	1	1								
U75,93,110	73	733W01708	IC, D-LATCH 74LS373	3	3								
U88,122	74	733W01642	IC, D F-F 74LS175	2	2								
10.0 U92	75	733W02221	IC, MICROPRO 18085A	1	1								
U102,103	76	733W01766	IC, MUX 74LS353	2	2								
U106	77	537P02281	IC, PROM 93427	1	1								
U124	78	537P02284	IC, PROM 93427	1	1								
U125	79	733W01662	IC, DCDR 74LS155	1	1								
U126	80	733W00318	IC, NAND 74S00	1	1								
10.0 U129	81	537P03029	IC, PROM 12716	1	NA								
10.0 U130	82	537P03030	IC, PROM 12716	1	NA								
10.0 U131	83	537P03700	IC, PROM 12716	1	NA								
10.0 U132	84	537P03032	IC, PROM 12716	1	1								
U138	85	537P02282	IC, PROM 93427	1	1								
Y1	86	733W01800	IC, 1.8432 MHz K1114A	1	1								
Y2	87	733W01802	IC, 16 MHz K1114A	1	1								
Y3	88	733W01801	IC, 6 MHz K1114A	1	1								
14.0	89	156P11270	TEST SPEC, IOP	REF	REF								
	90	156P12302	REWORK INSTRUCTIONS	REF	REF								
	91	117P10059	WIRE, 26 AWG	AR	AR								
C70	92	702W05918	CAP., 0.033, 100 V	1	1								

PROPRIETARY NOTE ON SHEET 1 APPLIES TO ALL SHEETS

TITLE		DWG. SIZE	DWG. NO. 140S2650X	SHEET REV D
PWB ASSEMBLY, IOP				
		A4	SHEET 3.2 OF	

PLEASE FILL IN COMPLETELY ABOVE DOUBLE LINES

XEROX <input type="checkbox"/> CR <input checked="" type="checkbox"/> ORLY		PROGRAM(S) 8010	PAGE 1 OF 3	CR ORLY # 026753
PART NUMBER 140326500 140327878	REV	PART NAME PWBA-IOP	NEXT ASSY	S/S NO
ORIGINATOR-LOCATION-PHONE-DATE LEN BRADY ES 39538 1/13/87		RESPONSIBLE DESIGN ENGINEER ROY OGUS		DEPT APPROVAL
END ITEM(S)	FIELD DISPOSITION <input type="checkbox"/> REPAIR BY REPLACEMENT <input checked="" type="checkbox"/> NONE <input type="checkbox"/> USE TILL DEPLETION <input type="checkbox"/> MANDATORY RETROFIT		REQUESTED CUT-IN IMMEDIATE	REPLACEMENT RATE
<input type="checkbox"/> BASE NO CHANGE <input type="checkbox"/> SUPERCESSION CHANGE	<input type="checkbox"/> EME AFFECTED <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO	<input type="checkbox"/> SAFETY AFFECTED <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO	MFG. CUT-IN IMMEDIATE	
<input type="checkbox"/> REVISION CHANGE				

PROBLEM STATEMENT (INCLUDE CONSEQUENCES OF FAILURE TO TAKE ACTION)

EXISTING 16K E-PROMS ARE NO LONGER
(733W01506)

BEING MANUFACTURED BY TEXAS INSTRUMENTS.

REQUEST ALLOW ESM TO USE 32K E-PROMS (733W01597)
IN LIEU OF SPECIFIED DEVICES.
PATTERN NOS. = 537P03029, 3030, 3032, & 3700.
(SEE ATTACHED MEMO)

Loaded 1/14/87

DATE TO SYS TEAM		PRIORITY	CLASS	TOOL NO COST
DISPOSITION	DATE	LIST AND ATTACH SUPPORTING DOCUMENTS		DELTA UMC
<input type="checkbox"/> REJECT	CR PKG NO			DOB APPROVAL
<input type="checkbox"/> ACCEPT	DATE 1/14/87			ENG <i>R Hansen for</i> <i>R Ogus 1/14/87</i>
<input checked="" type="checkbox"/> ACCEPT ORLY	DECISION DUE DATE			MFG <i>Len Brady 1/15/87</i>
<input type="checkbox"/> PENDING				SERVICE <i>MS Jones 1-14-87</i>
EXPLANATION OF DISPOSITION				PROD MGR
				CUSTOMER CONCURRENCE IF REQUIRED

Laurel Message

From: DRODGERS.ES

Date: Thu, 8 Jan 87 20:00 PST

Subject: 32K Masters

To: R. Dances M2-03<ESMail>

XEROX

Bob,

Relative to the note below, I have a set of master EPROM's that you may have if you want them for the four patterns.

DR.

Date: Fri, 19 Dec 86 13:19 PST

From: DRODGERS.ES

Subject: Substitute for 16K EPROM on 8010

To: Len Brady ESCG-237<ESMail>

cc: S. McMullen M4-06/ A. Ray A2-18<ESMail>, AKanadjian, DRodgers

This is a response to your request to find a solution to the lack of suppliers on the 733W01506 2KX8 EPROM that is used on the IOP board of 8010. We recommend that you replace this part with the 4KX8 EPROM 733w01597. We have reviewed the board design and the device specifications and found that there is no difference in the device pins for the two devices as used on the IOP except as follows:

Pin# / -1506 / -1597 / IOP board function
18/PDPGM/ CEbar / BankSelectbar
20/ CEbar /OEbarVPP/MemReadbar
21/ VPP / All / VCCtie

Pin 18 PDPGM or CEbar act in an identical way to select or powerdown the part.

Pin 20 CEbar and OEbarVPP act the same to turn on/off the outputs of the part.

Pin 21 The VCCtie for the -1597 merely causes only one half of the 32K part to be accessed if it is used on the IOP board.

We programmed two sets of four EPROMS using the -1597 32K device by putting the same 16K pattern in each half (All=0 and All=1) of the device. One set used TI parts and one used Fujitsu parts; the two qualified sources for the 32K. The devices were used to stuff two IOP's which were then tested on the GRboard tester and 8010 systems in M1 and M2; no failures occurred.

There should be no problem using the 32K device on the board as long as it is programmed correctly. Change Requests should be written against the four 537 pattern drawings to change the part no. from 733w01506 to 733w01597 and the test spec. no. from 156P16305 to 156P12575 and to change the data pattern as follows:

The first two pages of the data pattern should remain as is and two more pages should be added that are identical to the first except the four hex

addresses under the address column start at 0800 and count up to 0FE0 as they would for the last 16K bits of a 32K device.

The pattern #'s are: 537P03029, 537P03030, 537P03032, 537P03700.

Len, sorry for the delay in getting this to you, we had many high priority tasks recently.

DR.

cc:

ESC-1 ESCG-37CESMaid

DRodgers

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REVISION RECORD

DWG STATUS

CHG. NO.

REV

REV	TYPE	CHG BY/DATE	CHK BY/DATE	CHK CODE	CHG NO.	MF CHK
A	ISS	J. Adams 07 MAR 83			559788	ME
B	D/C	E. J. Parry 26 JUL 83	E. J. Parry 26 JUL 83	3	559794	ME

SHEET NO.	SIZE	SHEET REVISION						SHEET NO.	SIZE	SHEET REVISION					
0.2	A4							10	A4	A	B				
0.3	A4	A	B					11	A4	A	B				
0.4	A4	A	B					12	A4	A	B				
0.5	A4	A	B					13	A4	A	B				
0.6	A4	A	B					14	A4	A	B				
0.7	A4	A	B					15	A4	A	B				
01	A4	A	B					16	A4	A	B				
02	A4	A	B					17	A4	A	B				
03	A4	A	B					18	A4	A	B				
04	A4	A	B					19	A4	A	B				
05	A4	A	B					20	A4	A	B				
06	A4	A	B					21	A4	A	B				
07	A4	A	B					22	A4	A	B				
08	A4	A	B					23	A4	A	B				
09	A4	A	B					24	A4	A	B				

XEROX MATERIAL SPEC

XEROX FINISH SPEC

RELATED SPECS

PREPARED BY/DATE

CHECKED BY/DATE

APPROVED BY/DATE

REFERENCE CODES

Adams
27 FEB 82

E. J. Parry
5 MAR 82

D. Russell
30 MAR 82

TITLE

SCHEMATIC, IOP

DWG
SIZE
A4

DWG
NO. 156P11952
SHEET 0.1 OF 66

SEE
REV
RECORD
ABOVE

SHEET NO.	SIZE	SHEET REVISION						SHEET NO.	SIZE	SHEET REVISION					
25	A4	A	B					58	A4	A	B				
26	A4	A	B					59	A4	A	B				
27	A4	A	B												
28	A4	A	B												
29	A4	A	B												
30	A4	A	B												
31	A4	A	B												
32	A4	A	B												
33	A4	A	B												
34	A4	A	B												
35	A4	A	B												
36	A4	A	B												
37	A4	A	B												
38	A4	A	B												
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51	A4	A	B												
52	A4	A	B												
53	A4	A	B												
54	A4	A	B												
55	A4	A	B												
56	A4	A	B												
57	A4	A	B												

PROPRIETARY NOTE ON SHEET 1 APPLIES TO ALL SHEETS

TITLE SCHEMATIC, IOP	DWG. SIZE A4	DWG. NO. 156P11952 SHEET 0.2 OF	SHEET REV. (Record Above)
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SHEET

- 0.4 BLOCK DIAGRAM: I/O PROCESSOR DATA PATHS
 0.5 BLOCK DIAGRAM: I/O PROCESSOR CONTROL ORGANIZATION
 0.6 BLOCK DIAGRAM: FLOPPY CONTROLLER
 0.7 BLOCK DIAGRAM: CP - IOP PORT

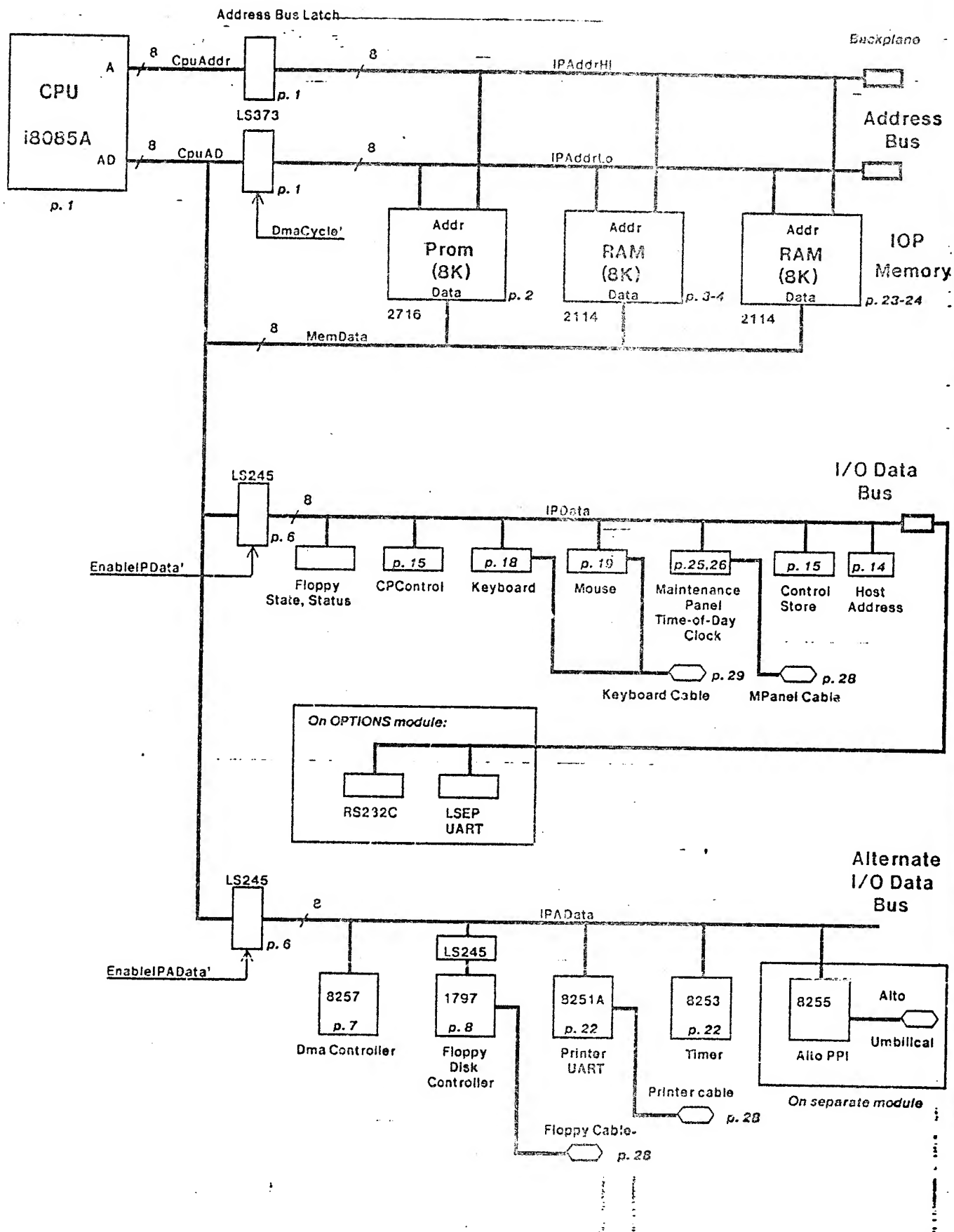
- 1 CPU
 2 PROM, MEMORY CONTROL
 3 4K RAM MEMORY BANKS 0 - 3
 4 4K RAM MEMORY BANKS 4 - 7
 5 I/O CONTROL, MEMORY CONTROL
 6 I/O DATA BUS CONTROL
 7 DMA CONTROLLER
 8 FLOPPY DISK CONTROLLER
 9 FLOPPY DISK CONTROLLER WRITE COMPARE
 10 FLOPPY DISK CONTROLLER MISCELLANEOUS
 11 FLOPPY DISK RECEIVERS/DRIVERS
 12 FLOPPY DISK CONTROLLER DATA SEPARATOR
 13 DMA TEST REGISTER
 14 INTERRUPT REQUEST REGISTER
 15 CP CONTROL, CONTROL STORE
 16 CP - IOP PORT - 1
 17 CP - IOP PORT - 2
 18 KEYBOARD INTERFACE
 19 MOUSE INTERFACE
 20 TIME-OF-DAY/MAINTENANCE PANEL INTERFACE
 21 MISCELLANEOUS CPU CONTROL
 22 PRINTER INTERFACE
 23 4K RAM MEMORY BANKS 8 - 11
 24 4K RAM MEMORY BANKS 12 - 15
 25 TIME-OF-DAY CLOCK - 1
 26 TIME-OF-DAY CLOCK - 2
 27 DISCRETES, I/O CONNECTORS - 1
 28 I/O CONNECTORS - 2
 29 FUSES, POWER SUPPLY, CONNECTORS
 30 BOOT AND RESET CIRCUITRY
 31 FILTER CAPACITORS
 32 SPARE COMPONENTS
 33 TEST POINT LISTING, CONNECTOR LISTING, SIGNAL LISTING

Note: The issued schematic drawing is made from [Rain]<SDMod>IOP3.dmASIL-C

TABLE OF CONTENTS

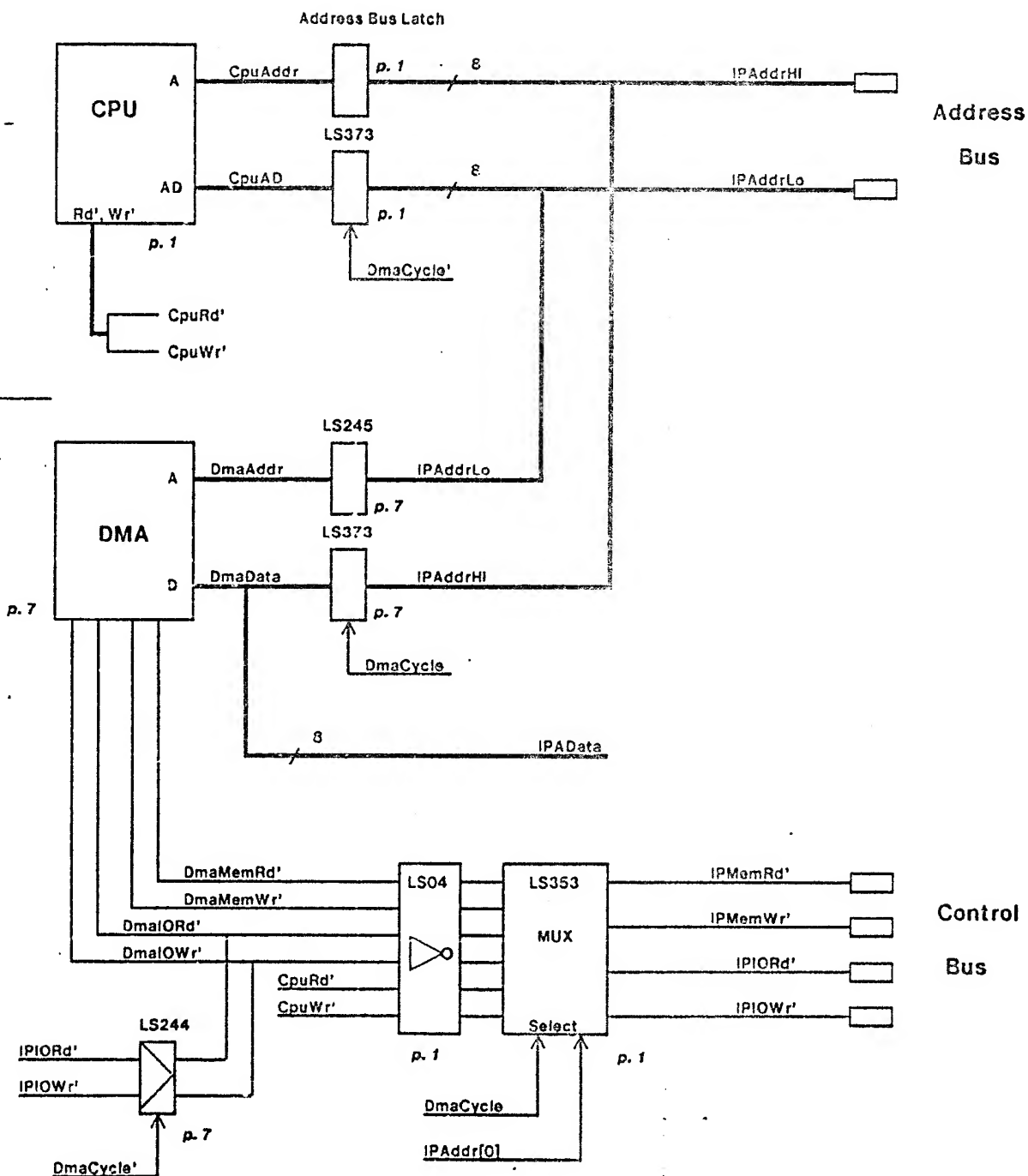
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE	SCHEMATIC, IOP		SHEET	0.3 OF	

Reference



BLOCK DIAGRAM: I/O PROCESSOR DATA PATHS

ROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP	Reference	A4	SHEET 0.4 OF	

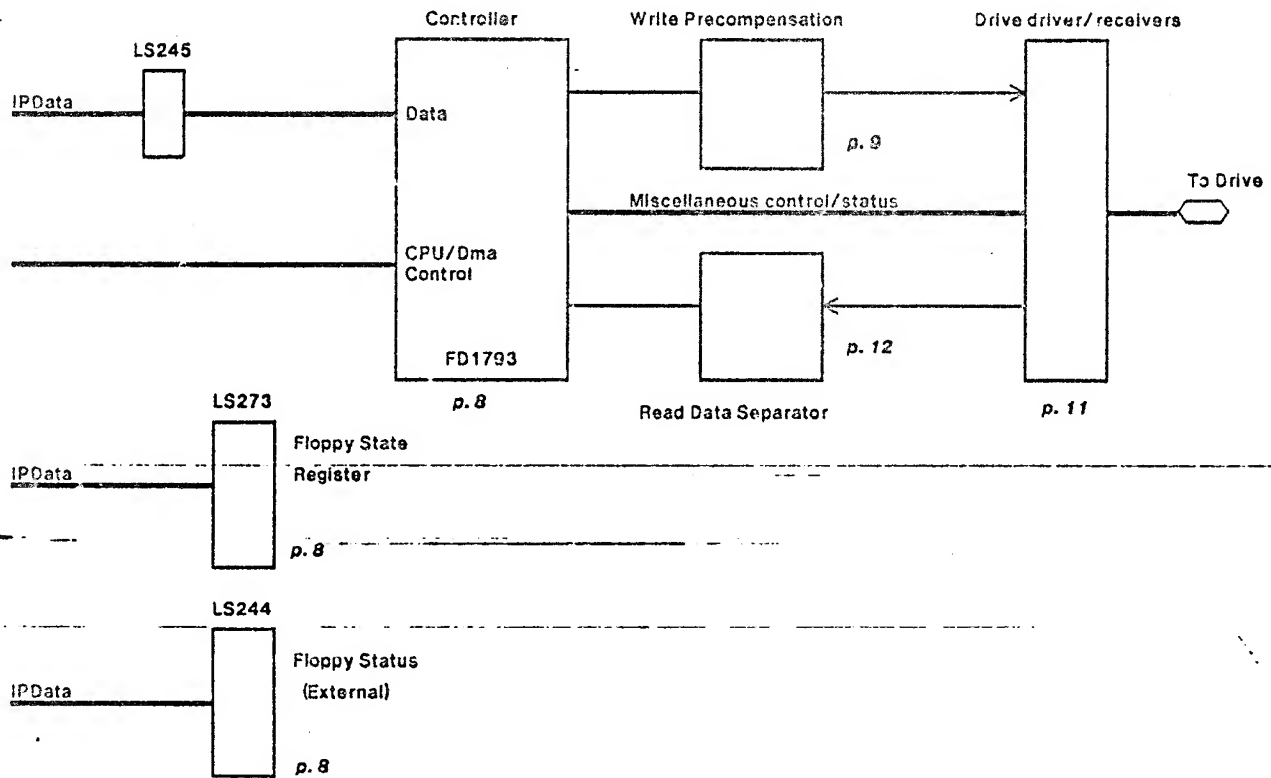


BLOCK DIAGRAM: I/O PROCESSOR CONTROL ORGANIZATION

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP <div>Reference</div>			SHEET 0.5 OF		

I/O Processor Floppy Disk Controller

Block Diagram



BLOCK DIAGRAM: FLOPPY CONTROLLER

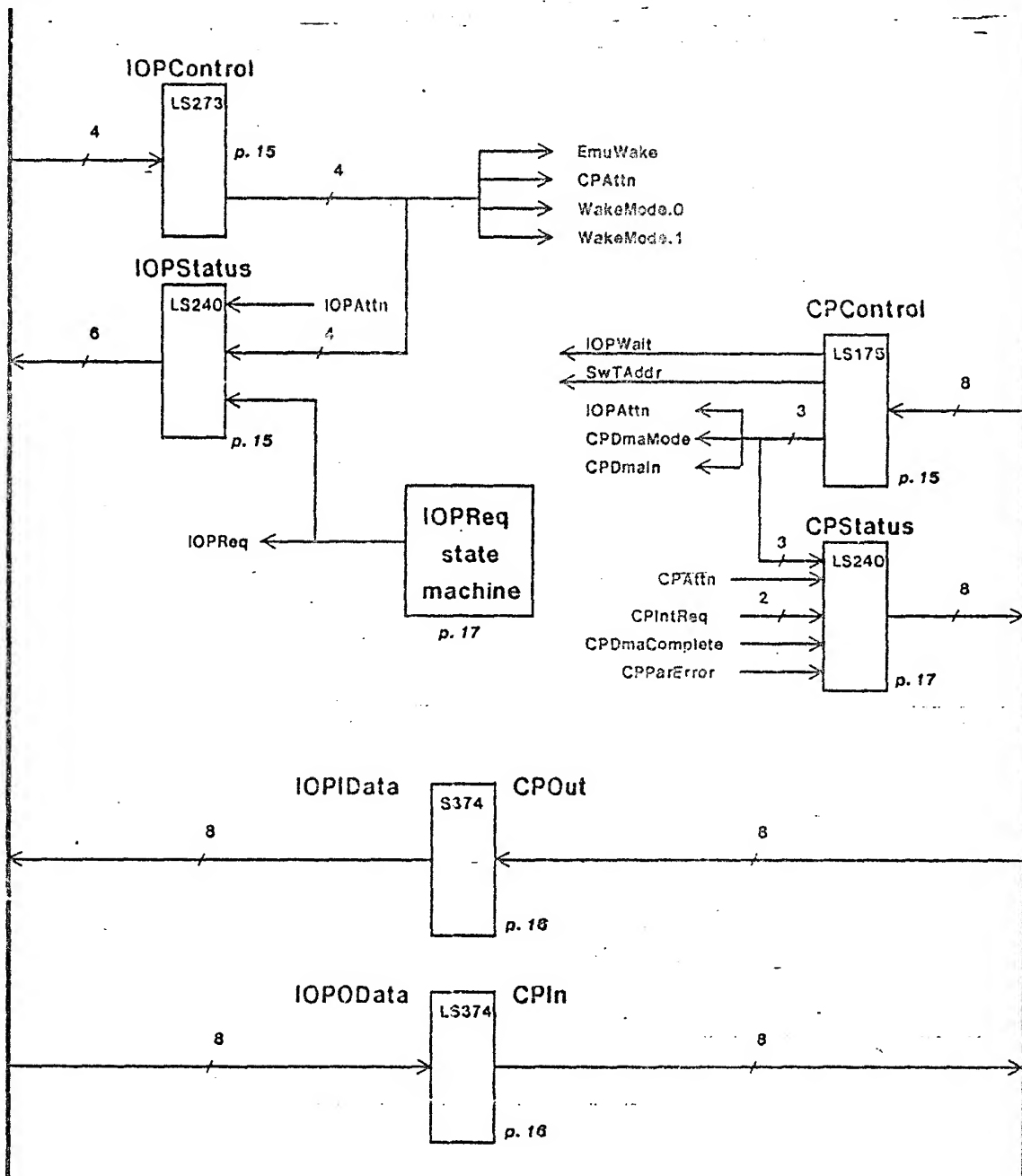
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE	SCHEMATIC, IOP		SHEET	0.6 OF	

Central Processor

I/O Processor

X-bus

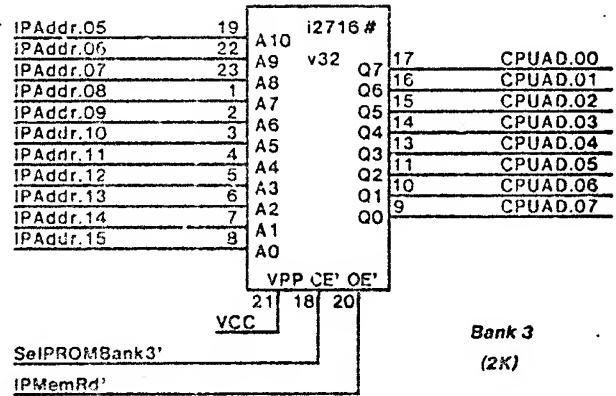
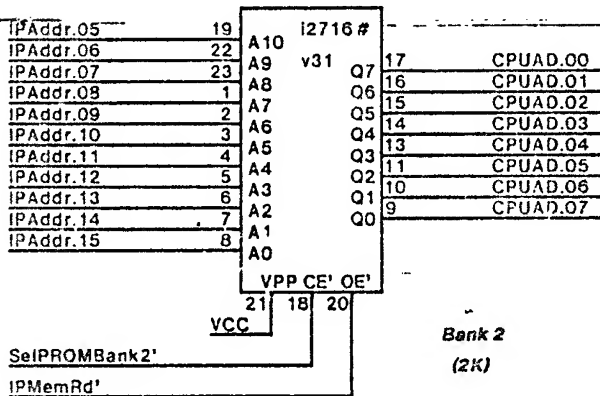
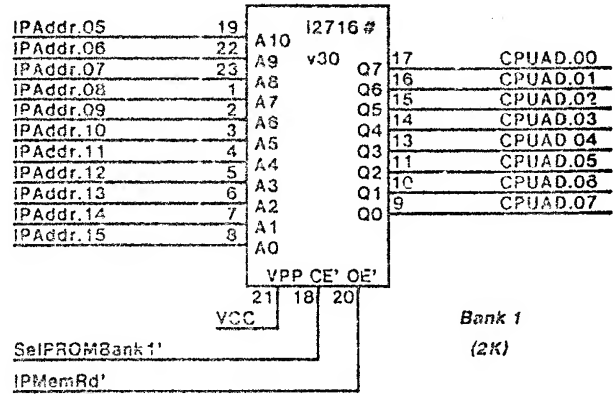
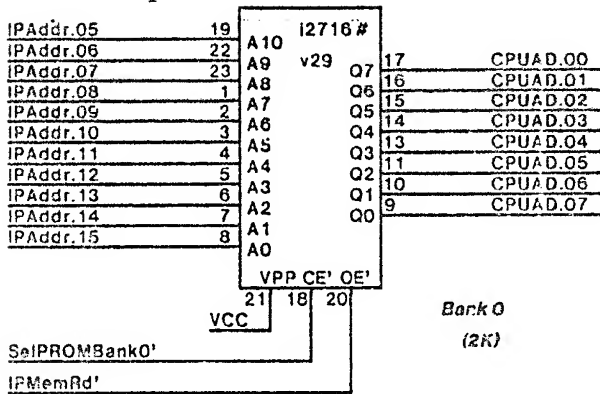
IOPData bus



BLOCK DIAGRAM: CP - IOP PORT

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE	DWG NO. 156P11952		SHEET REV.
	TITLE	SCHEMATIC, IOP	A4	SHEET 0.7 OF		
		Reference				B

Prom

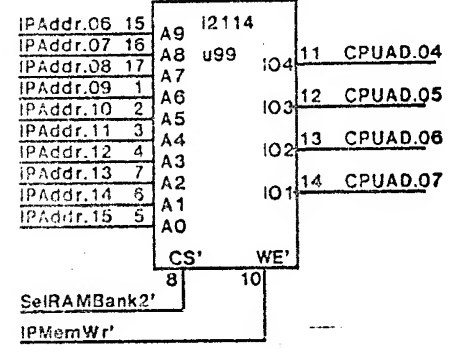
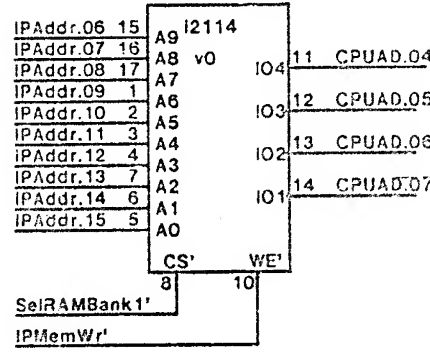
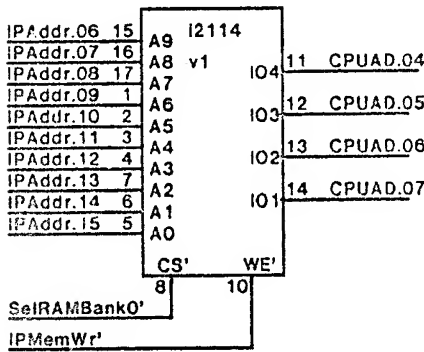
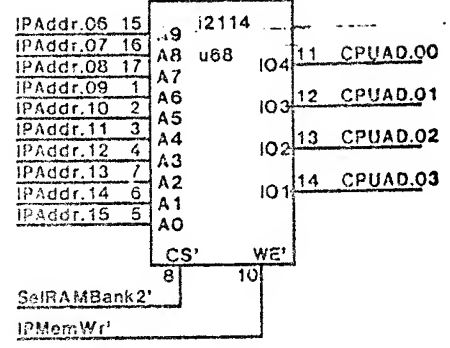
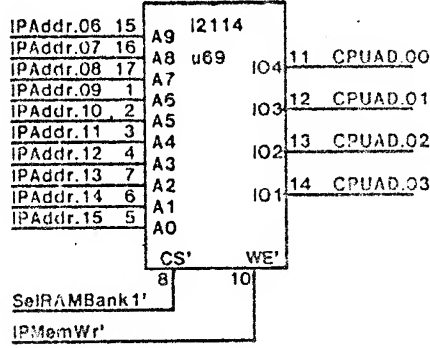
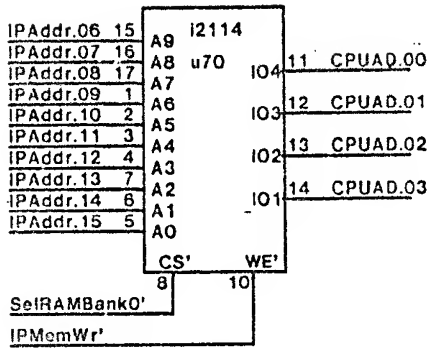


CPUAD.00	1	⊗	II	#TP3
CPUAD.01	1	⊗	II	#TP4
CPUAD.02	1	⊗	II	#TP5
CPUAD.03	1	⊗	II	#TP6
CPUAD.04	1	⊗	II	#TP7
CPUAD.05	1	⊗	II	#TP8
CPUAD.06	1	⊗	II	#TP9
CPUAD.07	1	⊗	II	#TP10

I/O Processor PROM

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 02 OF		

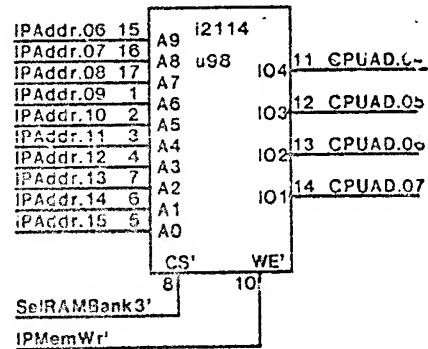
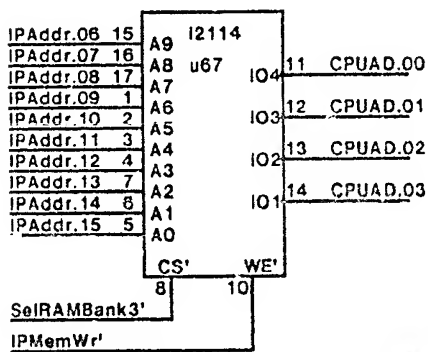
RAM - Banks 0 - 3



Bank 0

Bank 1

Bank 2

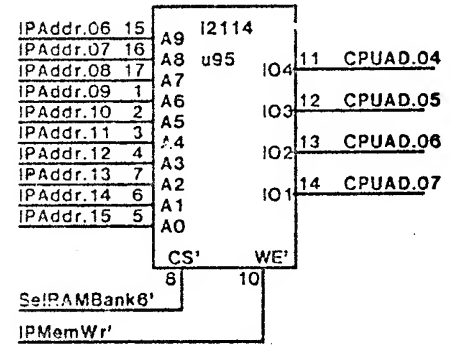
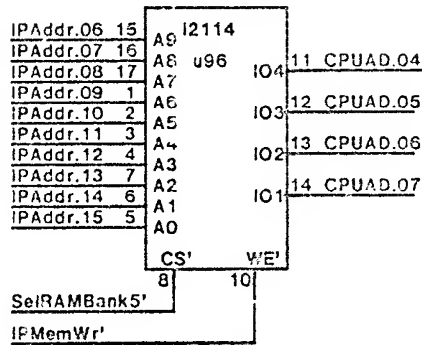
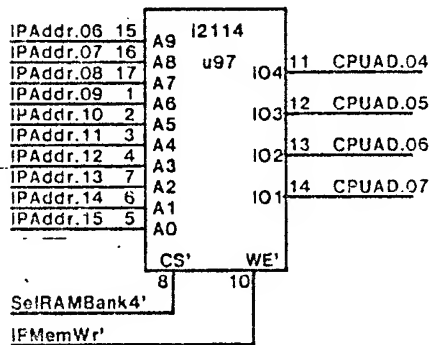
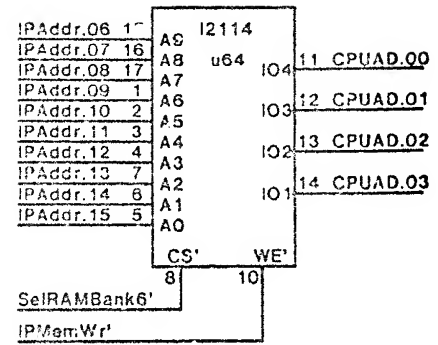
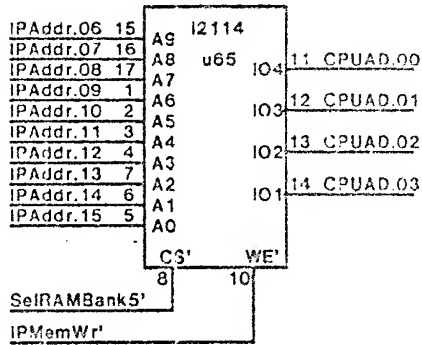
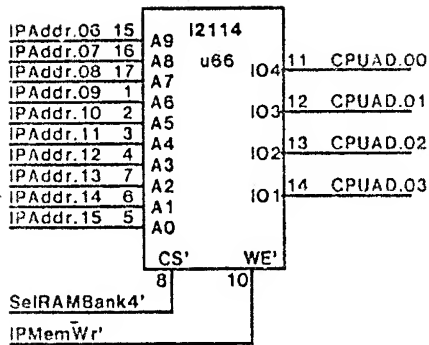


Bank 3

I/O Processor 4K RAM Memory-Banks 0-3

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 03 OF		

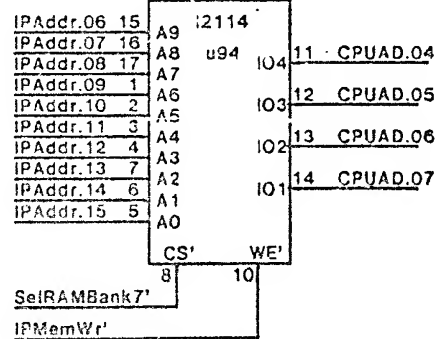
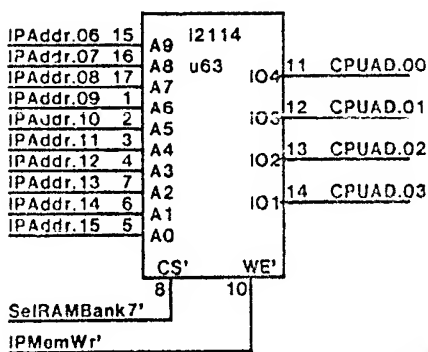
RAM - Banks 4 - 7



Bank 4

Bank 5

Bank 6



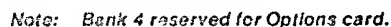
Bank 7

Note: RAM Banks 8 - 15 on pages 23 and 24.

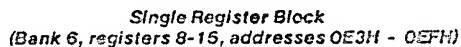
I/O Processor 4K RAM Memory-Banks 4-7

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIED TO ALL SHEETS		DWG NO. 156P11952	SHEET REV. B
	TITLE	SCHEMATIC, IOP		
		DWG SIZE A4	SHEET 04 OF	

(Depends on Addr[0] = Addr[8], etc. for I/O. IAddr[0] = 1 for I/O addresses.)



Note: Bank 5 is used by IPData bus test register.



The diagram shows the pin connections for two LS138 decoders, v45 and v46. Decoder v45 has inputs for GND (pin 3), IPAddr.03 (pin 2), and IPAddr.04 (pin 1). Its outputs are connected to TP121 through TP124. Decoder v46 has inputs for IPAddr.03 (pin 3), IPAddr.04 (pin 2), and IPAddr.05 (pin 1). Its outputs are connected to TP125 through TP132. Both decoders have additional inputs for IPAddr.01, IPAddr.00, and IPAddr.02, and a common input for IPMemRdWr'.

LS138 v45 Connections:

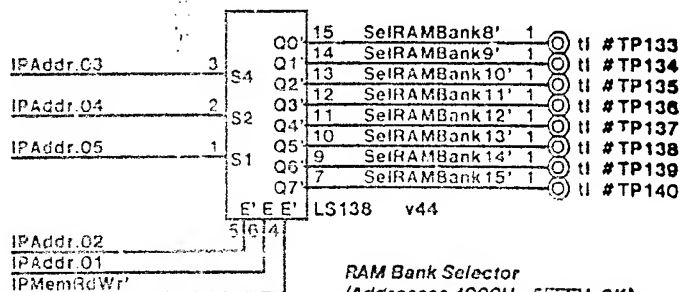
- Pin 3: GND
- Pin 2: IPAddr.03
- Pin 1: IPAddr.04
- Pin 15: SelPROMBank0' 1
- Pin 14: SelPROMBank1' 1
- Pin 13: SelPROMBank2' 1
- Pin 12: SelPROMBank3' 1
- Pin 11: TP121
- Pin 10: TP122
- Pin 9: TP123
- Pin 8: TP124
- Pin 7: TP125
- Pin 6: TP126
- Pin 5: TP127
- Pin 4: TP128
- Pin 3: TP129
- Pin 2: TP130
- Pin 1: TP131
- Pin 0: TP132

LS138 v46 Connections:

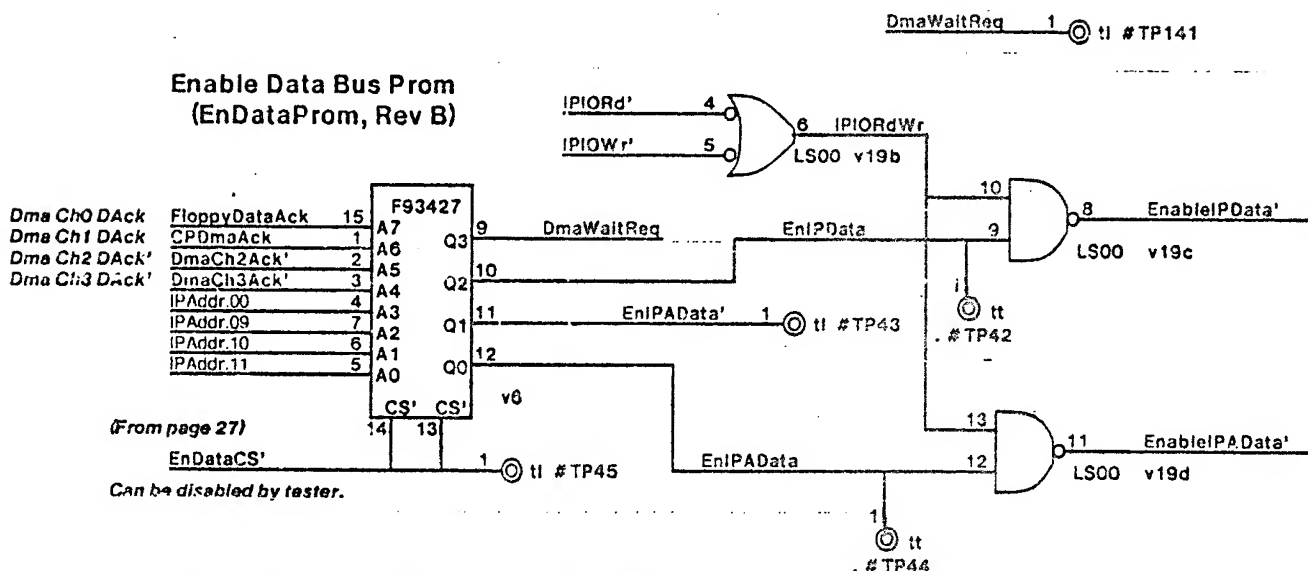
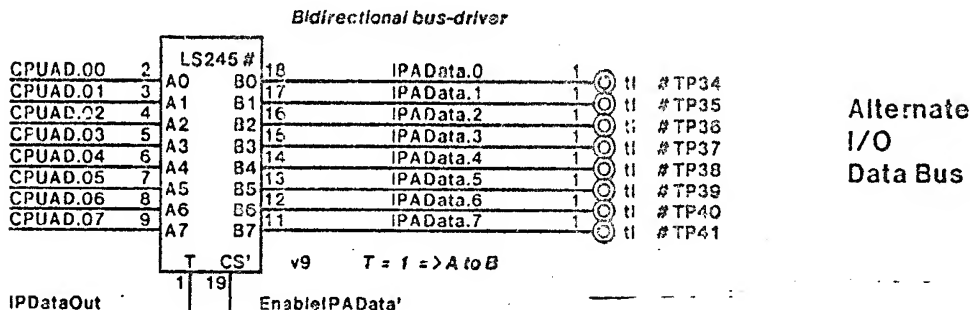
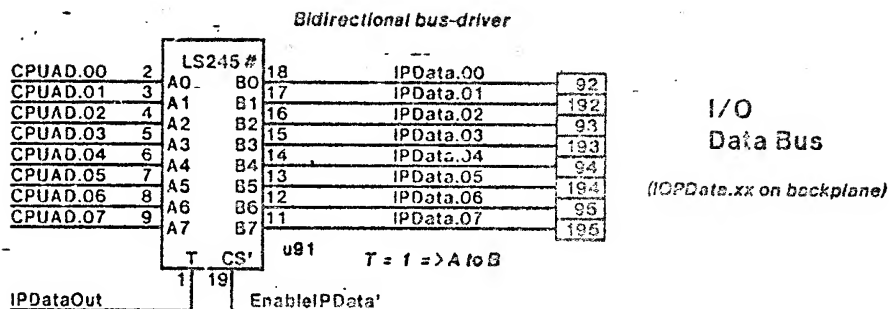
- Pin 3: IPAddr.03
- Pin 2: IPAddr.04
- Pin 1: IPAddr.05
- Pin 15: SelRAMBank01
- Pin 14: SelRAMBank11
- Pin 13: SelRAMBank21
- Pin 12: SelRAMBank31
- Pin 11: SelRAMBank41
- Pin 10: SelRAMBank51
- Pin 9: SelRAMBank61
- Pin 8: SelRAMBank71
- Pin 7: TP125
- Pin 6: TP126
- Pin 5: TP127
- Pin 4: TP128
- Pin 3: TP129
- Pin 2: TP130
- Pin 1: TP131
- Pin 0: TP132

PROM Bank Selector
(Addresses Bank 0: 0 - 7FFH,
Bank 1: 800H - 0FFFH,
Bank 2: 1000H - 17FFH,
Bank 3: 1800H - 1FFFH)

RAM Bank Selector
(Addresses 2000H - 3FFFH, 8K)



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 05 OF	



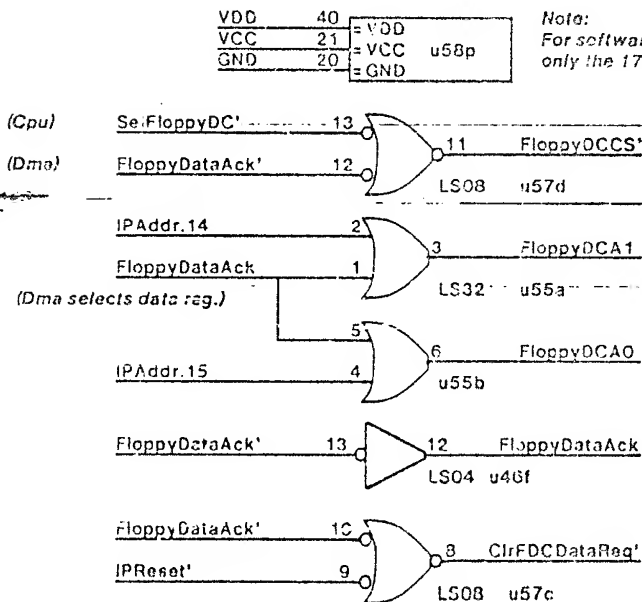
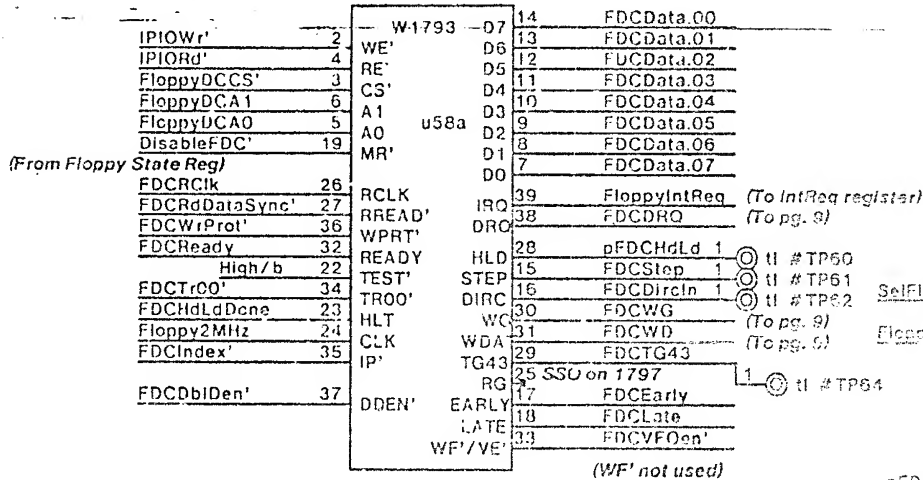
Note: Do not use DMA memory addresses in the I/O Address space.

I/O Processor I/O Data Bus Control -

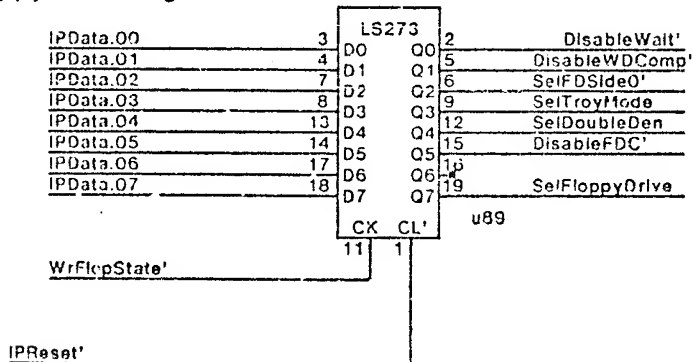
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP		A4	SHEET 05 OF	B

Floppy Controller

FloppyDataReq
FloppyIntReq) are pulled up
FDCVFOen'



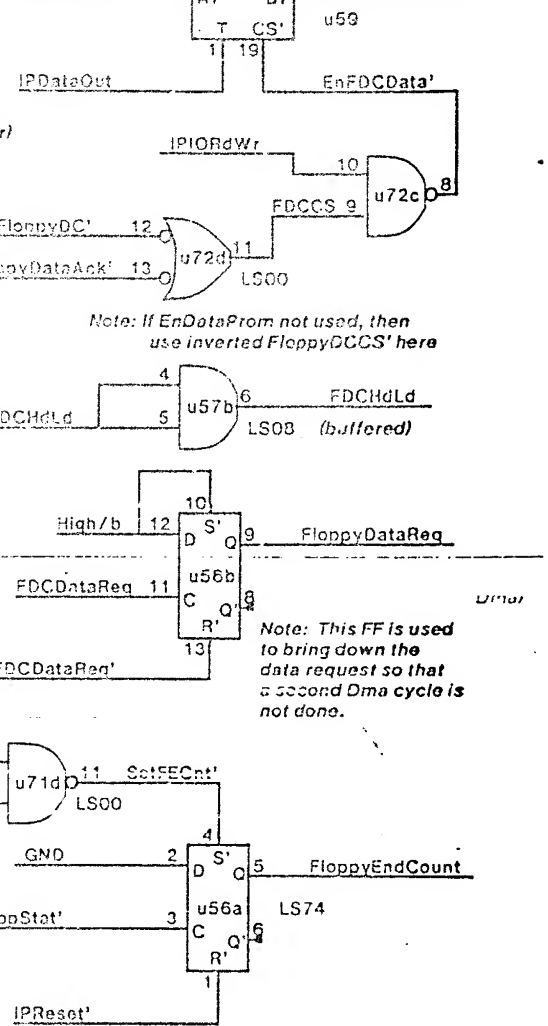
Floppy State Register



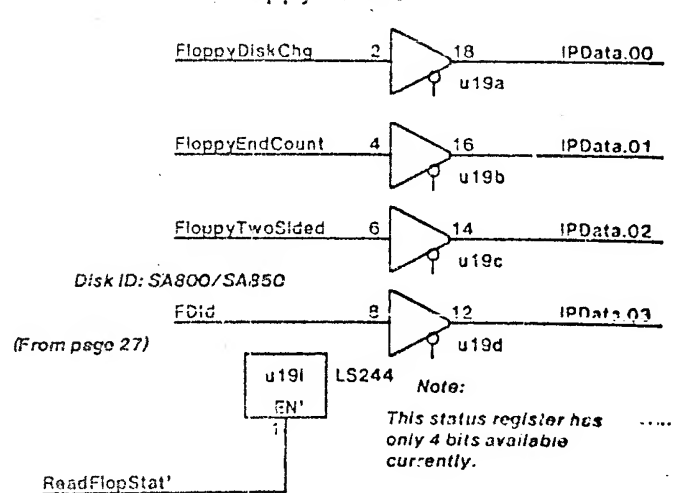
State register format:

- | | |
|------------------------------|----------------------------------|
| Bit 0 - Enable Cpu Waits | Bit 4 - Select Double Density |
| Bit 1 - Enable Write PreComp | Bit 5 - Enable Floppy Controller |
| Bit 2 - Select Side 1 | Bit 6 - (unused) |
| Bit 3 - Select Troy mode | Bit 7 - Enable Floppy Drive |

IPData.0	2	LS245 #	18	FDCData.00
IPData.1	3	A0	B0	FDCData.01
IPData.2	4	A1	B1	FDCData.02
IPData.3	5	A2	B2	FDCData.03
IPData.4	6	A3	B3	FDCData.04
IPData.5	7	A4	B4	FDCData.05
IPData.6	8	A5	B5	FDCData.06
IPData.7	9	A6	B6	FDCData.07



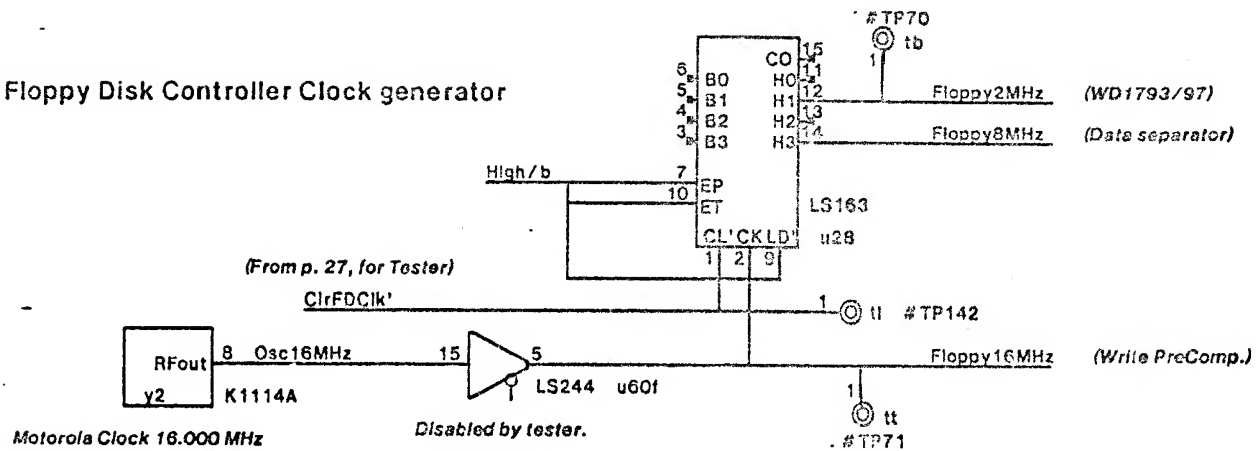
Floppy Status



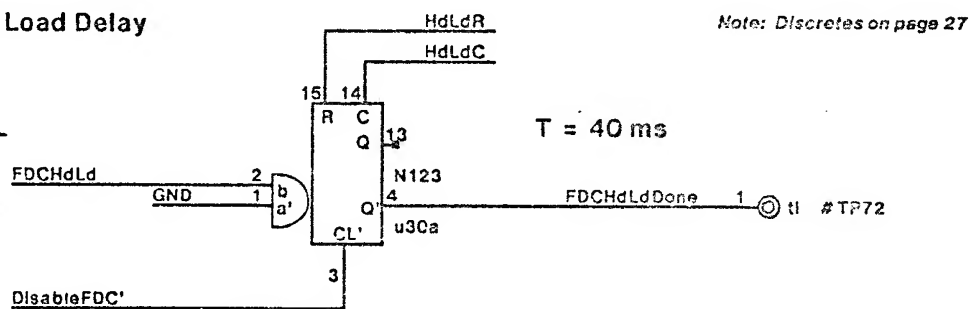
I/O Processor Floppy Controller

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE	DWG NO. 156P11952	SHEET REV. B
	TITLE	SCHEMATIC, IOP	A4	SHEET 08 OF	

Floppy Disk Controller Clock generator



Head Load Delay

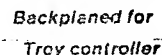


I/O Processor Floppy Controller Miscellaneous

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 10 OF		

**Backplaned for
Troy controller**

To FD cable
(page 28)



Note 4: TP 076 above is to be used to provide High/a signal when EnFDCIn' is inactive.

SelfFloppyDrive 2 18 FDSelDrive1'

register 4 16 FDInUse1'

SelfFDSideO1 6 14 FDSelSideO

u17a

u17b

u17c

u17d S240

EN'

Note: Schottky

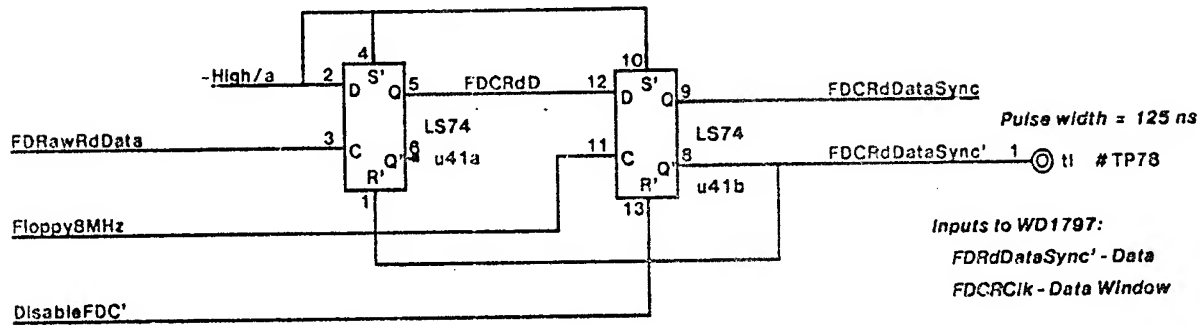
(Gate d used by Bell)

GND

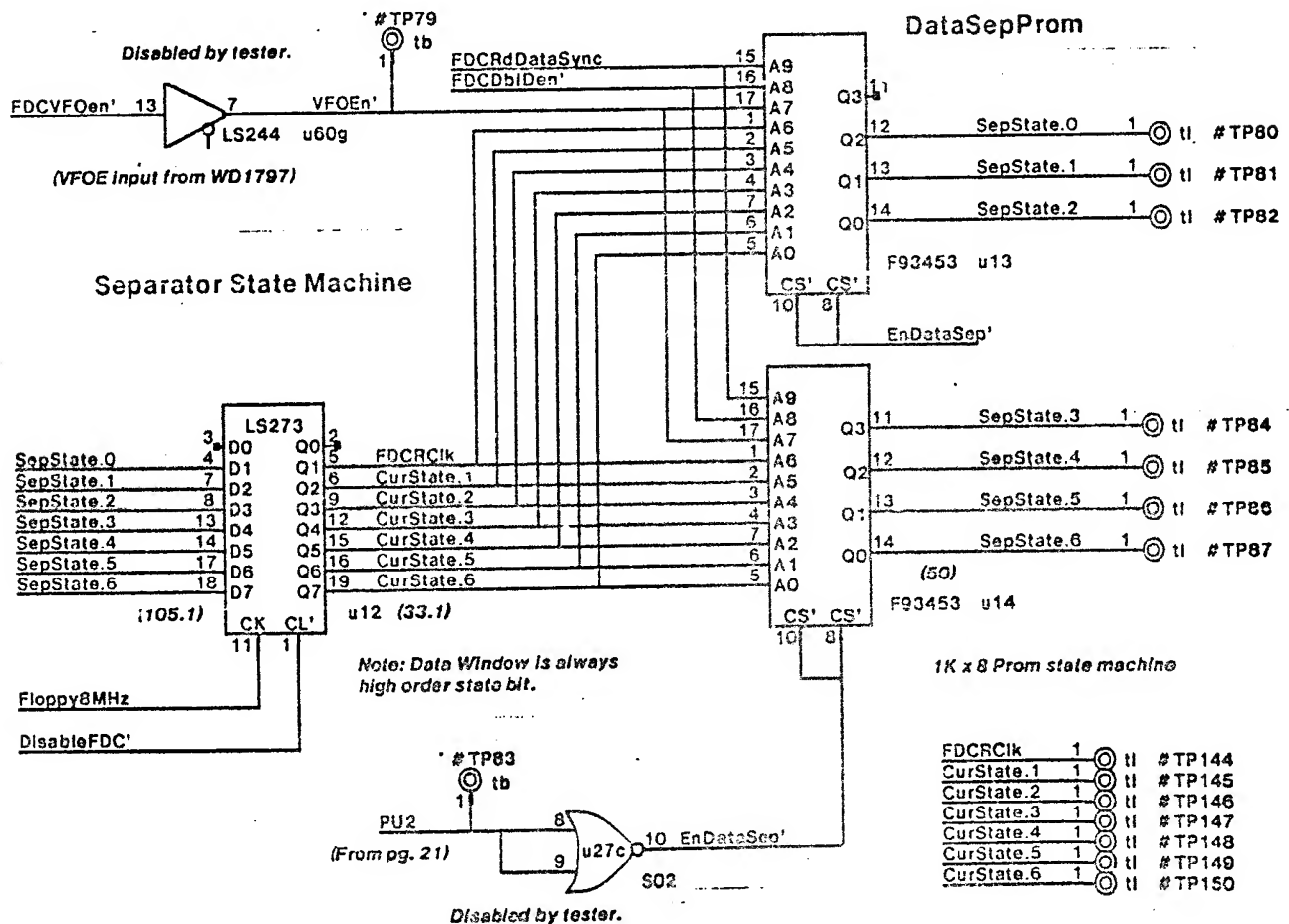
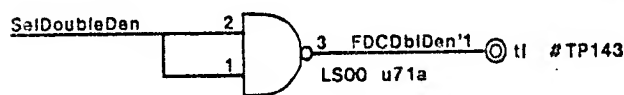
I/O Processor Floppy Disk Receivers/Drivers

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 11 OF	

Raw Read Data synchronizer and pulse shaper



Double density selection



I/O Processor Floppy Data Separator-

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
			SHEET 12	OF	

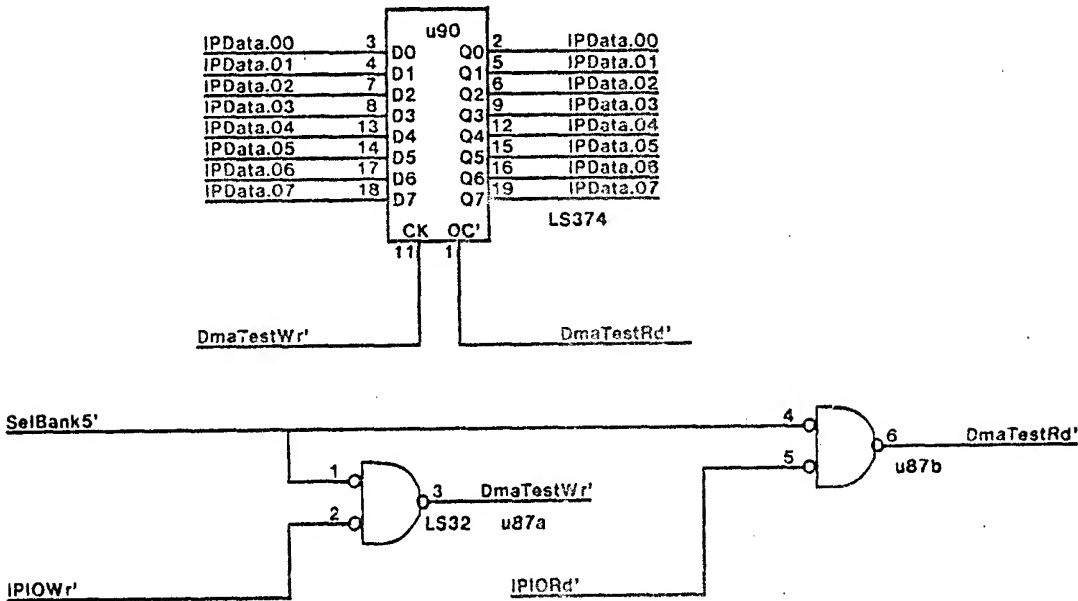
TITLE SCHEMATIC, IOP

IPData bus Test

This register can be used to test the integrity of the IPData bus, which is the external data bus.

The register can be written and then read back to determine the soundness of the bus.

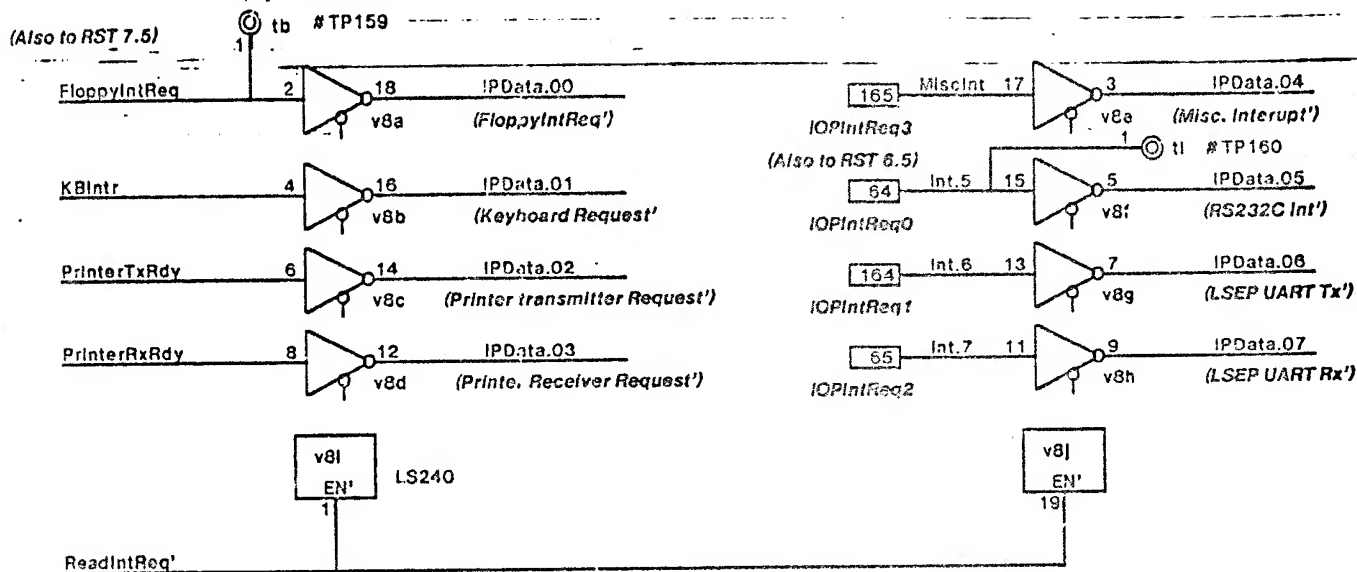
This register uses SelBank5' to enable it.



I/O Processor IPData bus Test

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE	DWG NO. 156P11952		SHEET REV.
	TITLE SCHEMATIC, IOP		A4	SHEET 13	OF	

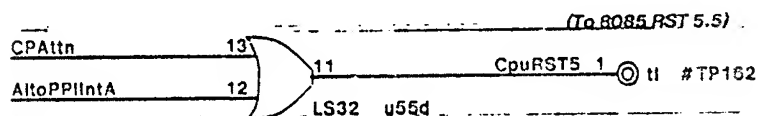
Interrupt Request Register



This register contains the interrupt requests of various devices.

To read true value of the requests, XOR with XOR vector = 1111 1111 (OFFH)

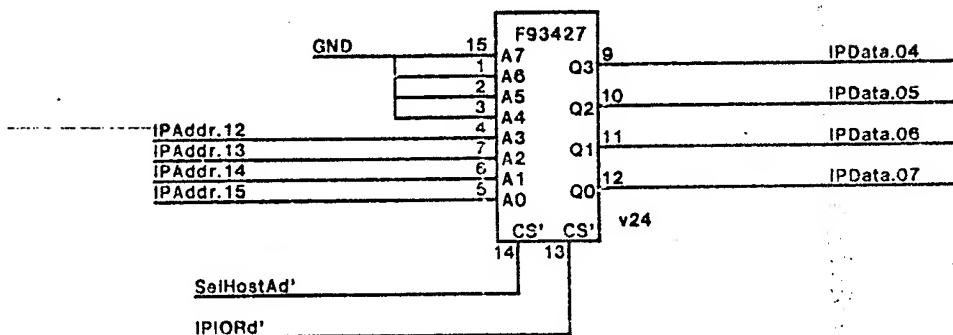
IOIntReq0 - RS232C - Options
IOIntReq1 - LSEP UART Tx - Options
IOIntReq2 - LSEP UART Rx - Options
IOIntReq3 - Miscellaneous interrupt (from Timer)



RST 5.5 interrupt is for MouseHalt or CPAttn

Host Address Prom

(HostAddrProm)



Host address is 48 bits long, stored in addresses 0 - 11 of the Prom.

Address 12, 13 contains an 8-bit checksum, 14, 15 contains the complement of the checksum.

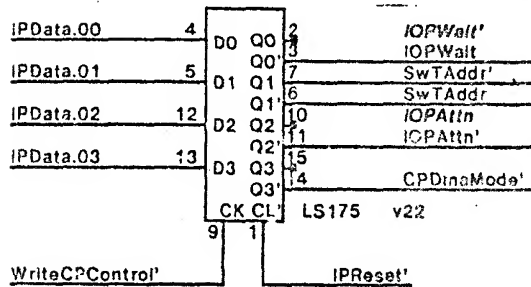
Host address Prom has the 16 I/O Bank 3 addresses.

I/O address	Host address bits
OB0H	0:3
OB1H	4:47
OB2H, OB3H	checksum
OB4H, OB5H	checksum'

I/O Processor Interrupt Req. reg, Host address

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 14 OF	

Central processor control CP port control

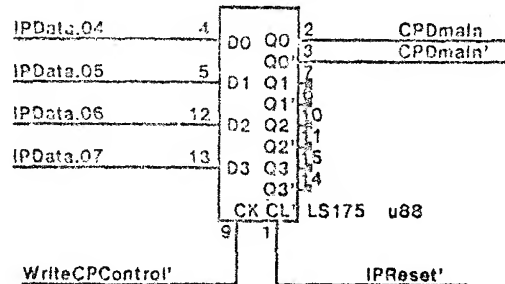


(IOPWait and SwAddr should be true after booting)

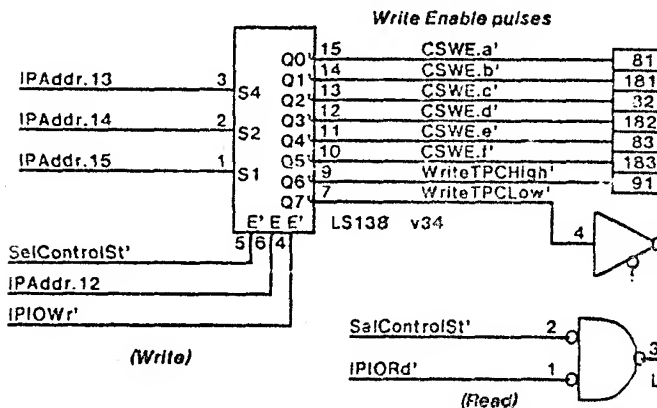
Date:

- Bit 0 - Enable CP (remove Wait)
- Bit 1 - Switch TPC address from MIAx
- Bit 2 - Set CP Attention
- Bit 3 - Set Dma Mode for CP port
- Bit 4 - Set Dma Mode for CPport as Input/output'

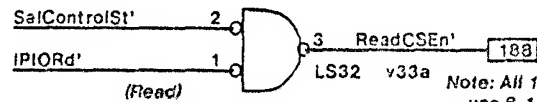
Normal state of register is 1100 0xxx



Control Store handling

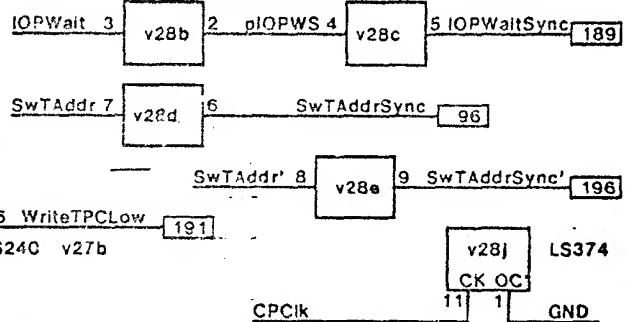


(Write)



(Bank 7, registers 8-15, addresses 0F8 - 0FFh)

CP synchronization

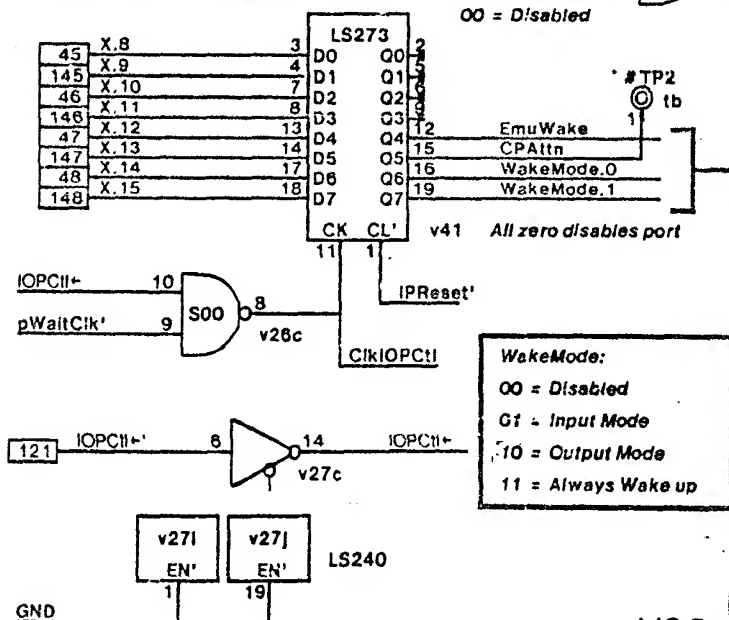


Note: All 16 addresses will respond for Read, use 8-15.

Central Processor registers

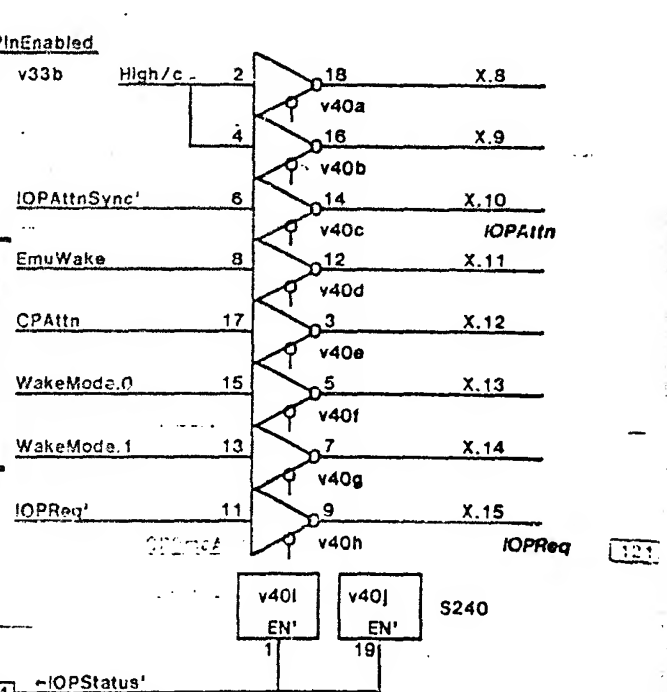
IOP Control

Note: Mesa should do a read-modify-write to set EmuWake



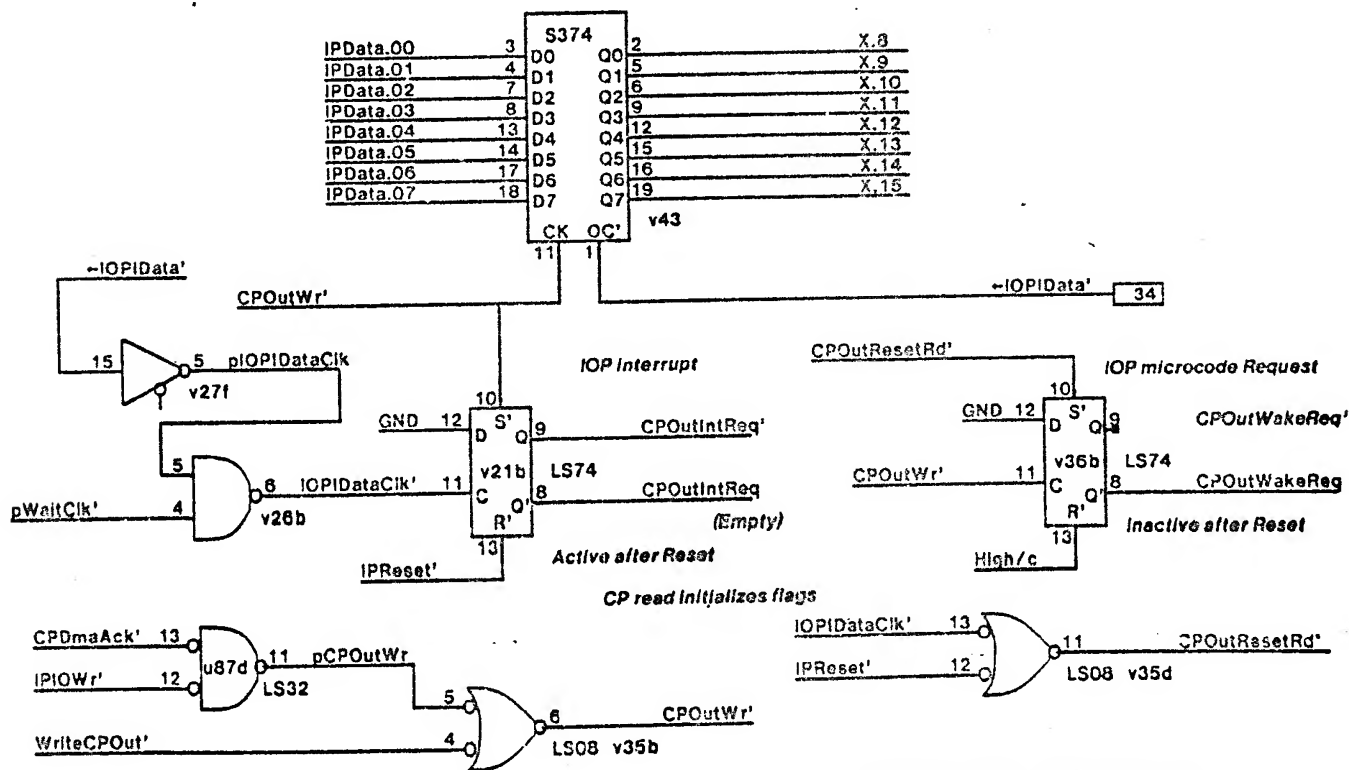
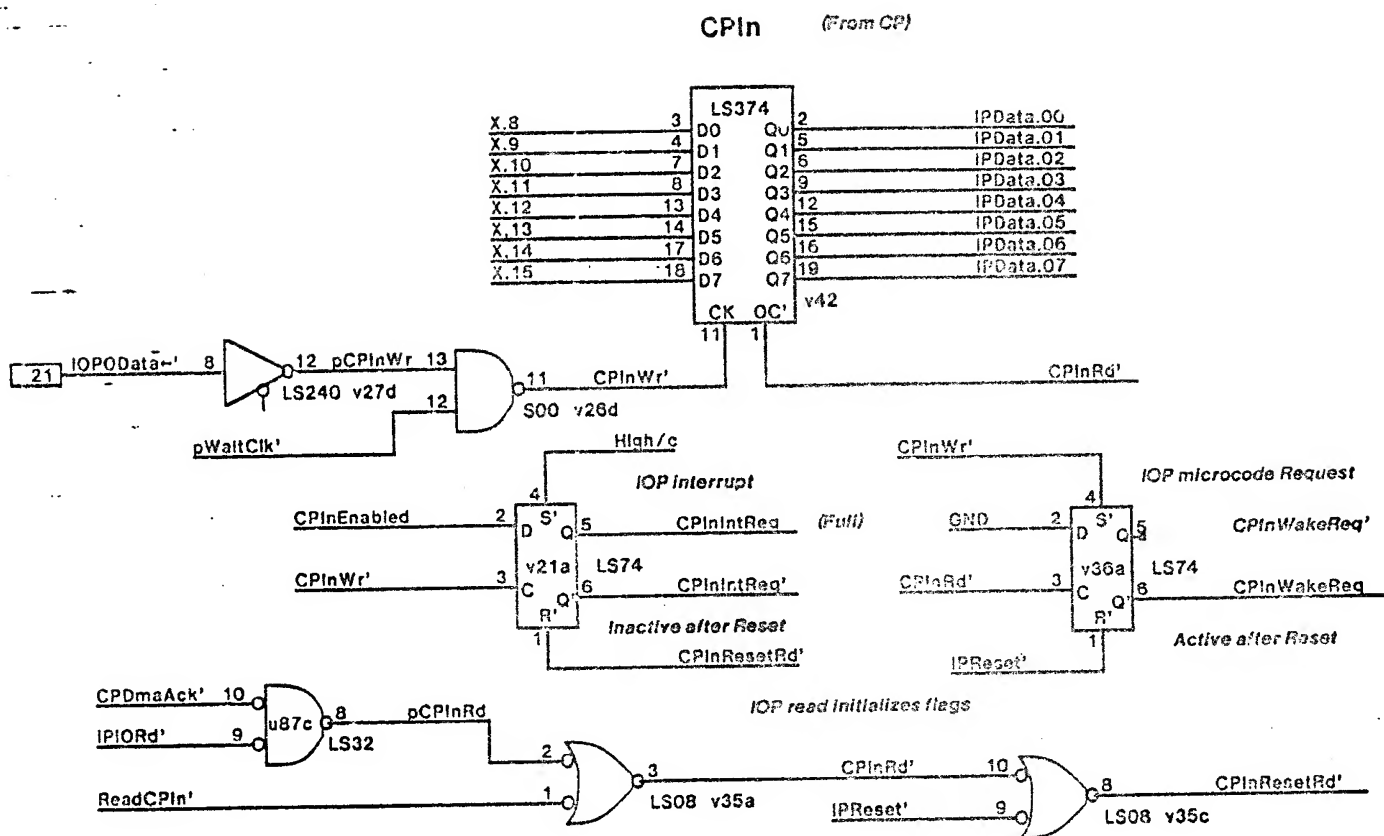
WakeMode:
00 = Disabled
01 = Input Mode
10 = Output Mode
11 = Always Wake up

IOP Status



I/O Processor CP Control and Control Store

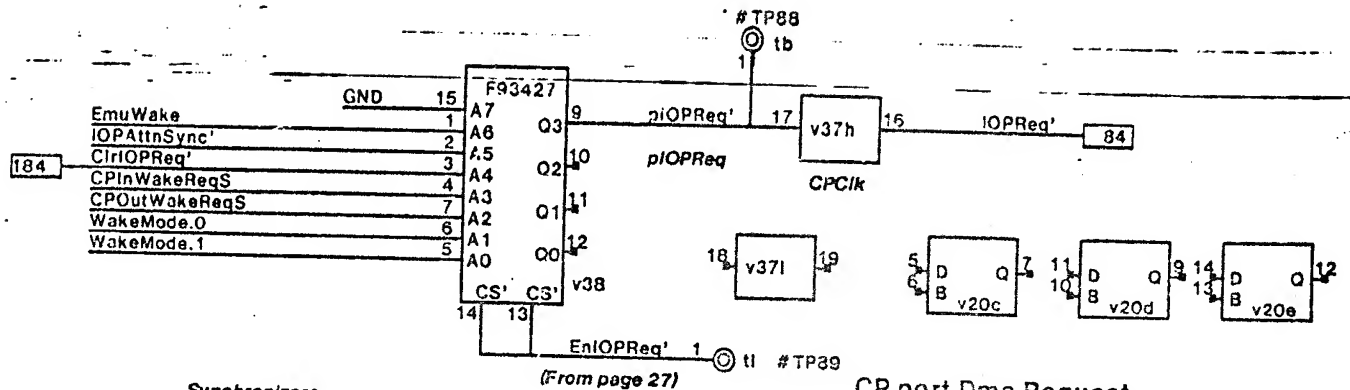
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE	SCHEMATIC, IOP		SHEET 15 OF		



I/O Processor CP-IOP port

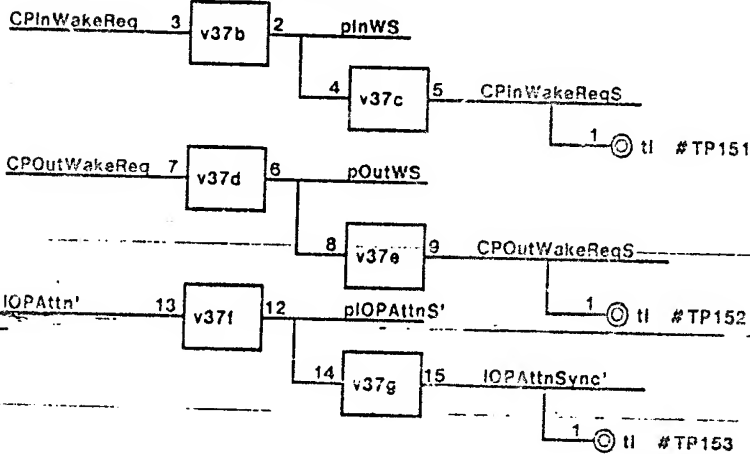
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 16 OF		

IOPReq



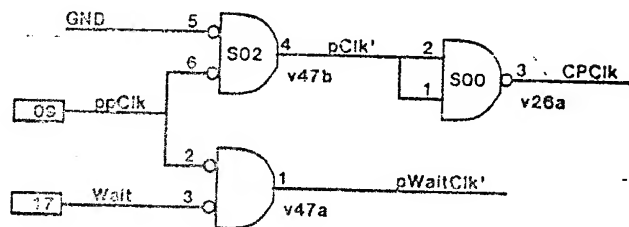
Synchronizers

CP port Dma Request



Note: First set up CPDmaIn, then CPDmaMode

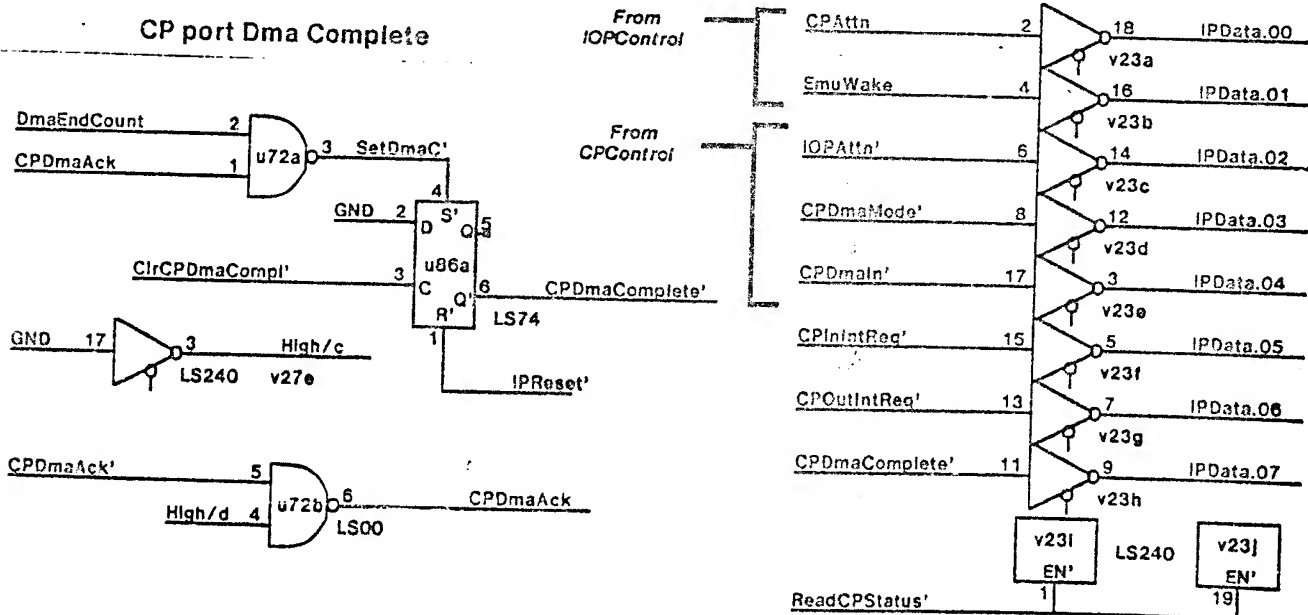
CP Clock



CP port status

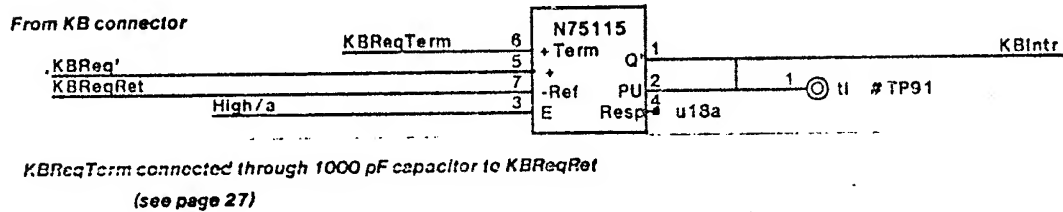
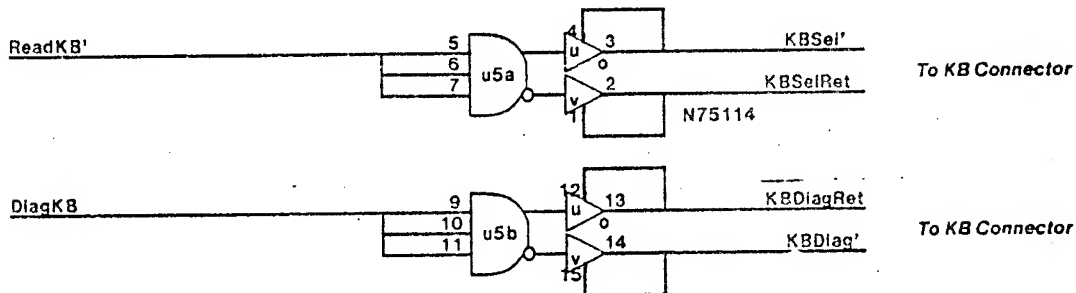
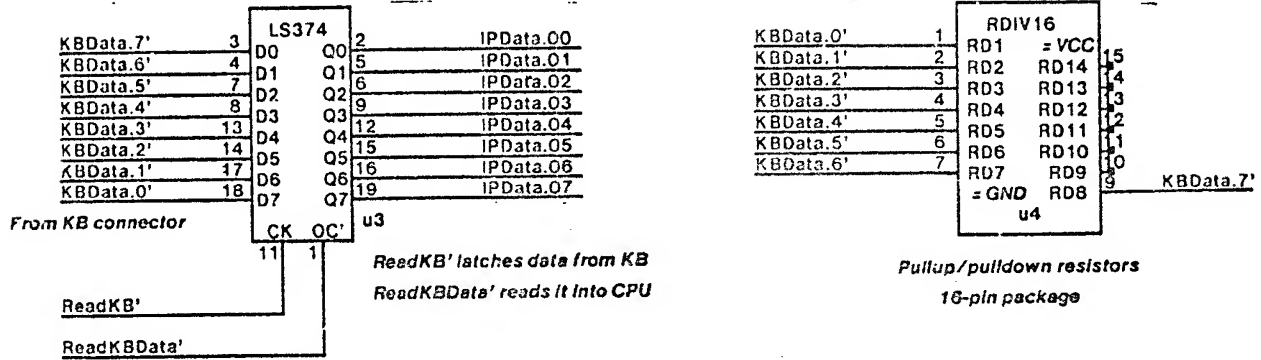
Also to I8095 RST 5 (with MouseHalt)

CP port Dma Complete



I/O Processor CP-IOP port - 2

Keyboard Data

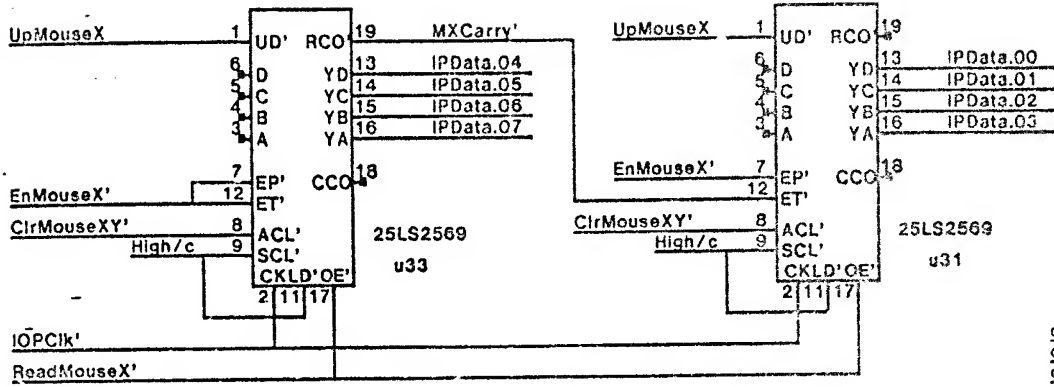


Bell circuit on page 27.

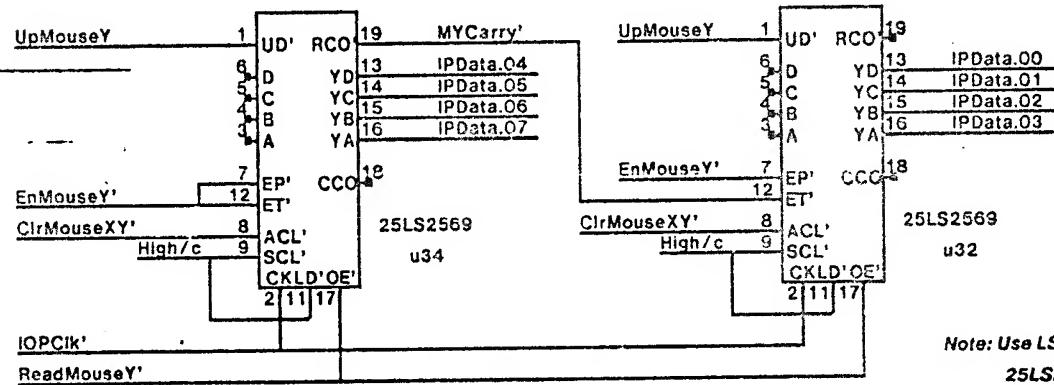
I/O Processor Keyboard Interface

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC. IOP			SHEET 18 OF		

X-coordinate



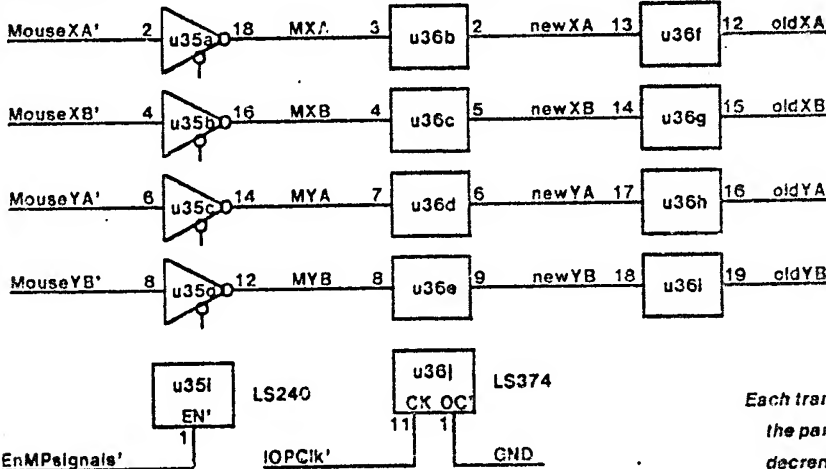
Y-coordinate



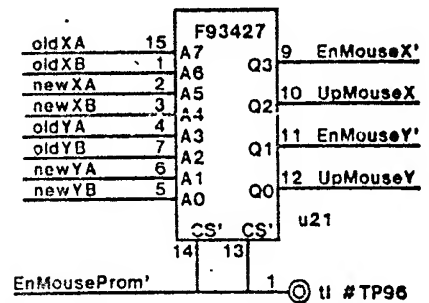
From KB connector

New sample

Old sample



MouseProm



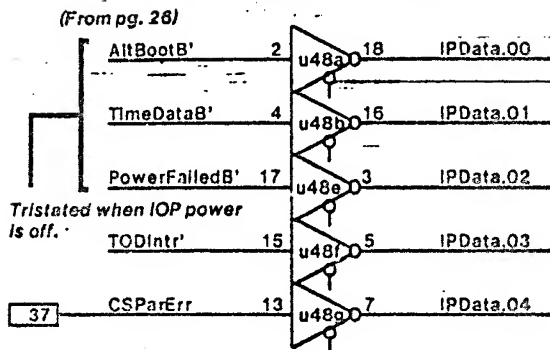
Each transition of XA or XB (YA or YB) causes the particular counter to be incremented or decremented. The samples are made with the inverted processor clock to ensure that the counters are stable when a read or clear of the counters is done.

ST (Note: u35 is powered by MVcc.
This signal tristates outputs
during power down.)

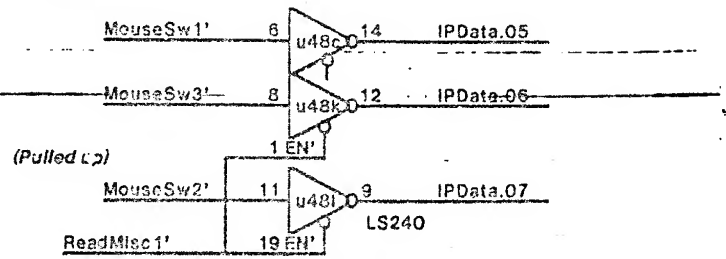
I/O Processor Mouse interface

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 19 OF		

Miscellaneous Input 1

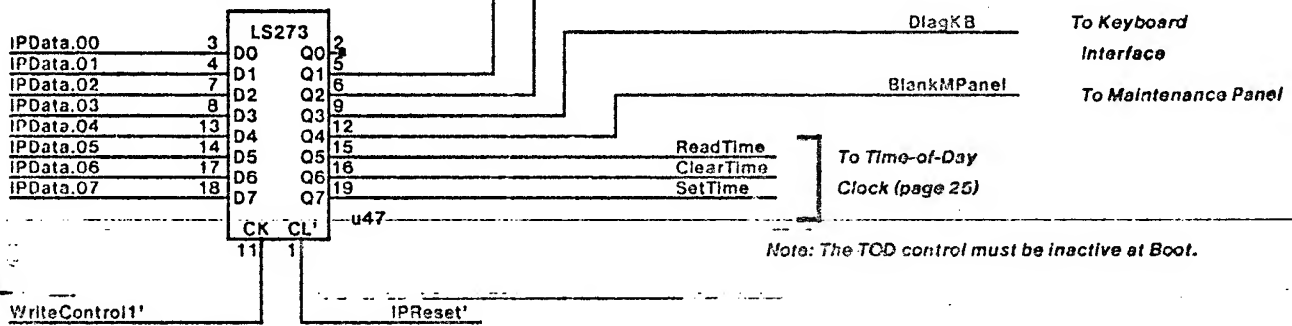


From KB connector

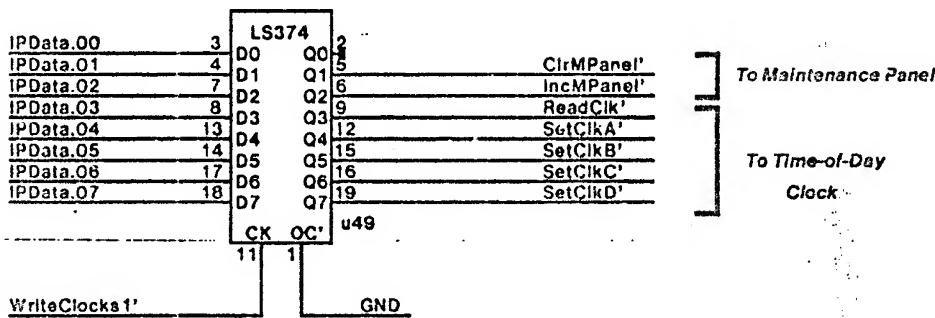


Note: For two-button mice, MouseSw2 does not exist.

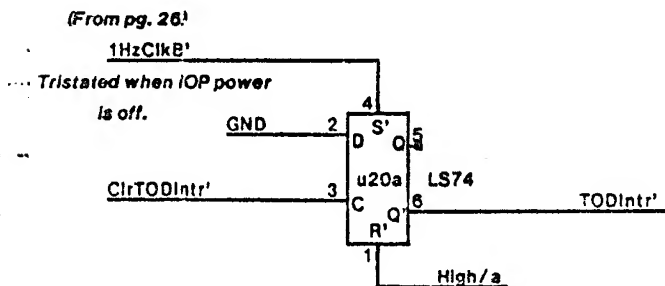
Miscellaneous control 1



Miscellaneous Clocks 1



Time-of-Day 1 second interrupt



Procedure to read time:

- Wait for TODIntr to be set
 - When set, clear and wait for it to be set again
 - read time
- (maximum delay = 2 seconds)

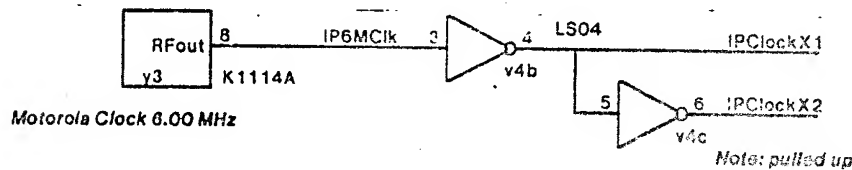
Alternative:

- clear TODIntr (if being set will not be cleared)
 - wait until set
 - read time
- (maximum delay = 1 second)

I/O Processor TOD/MP interface, misc. reg.

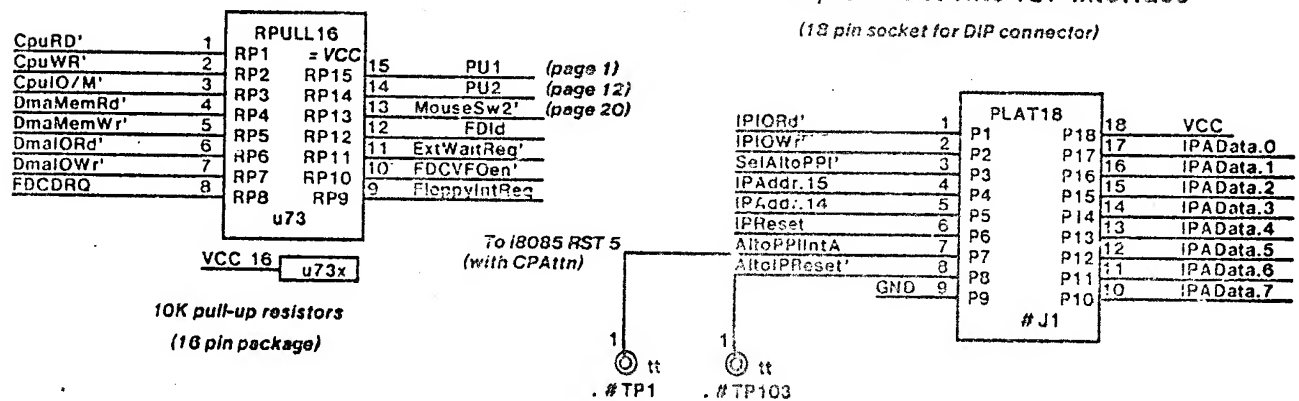
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 20 OF		

IOP CPU Clock generator



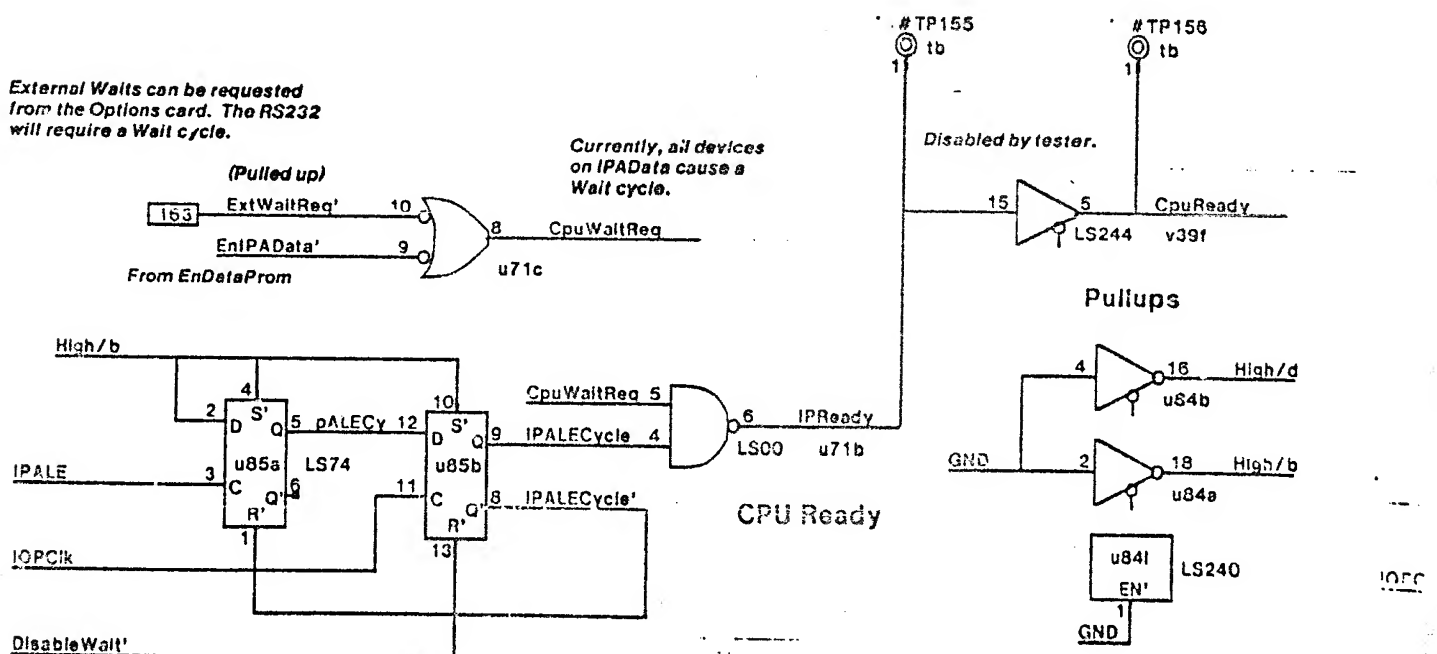
Dip Cable to Alto-IOP interface

(18 pin socket for DIP connector)



External Waits can be requested from the Options card. The RS232 will require a Wait cycle.

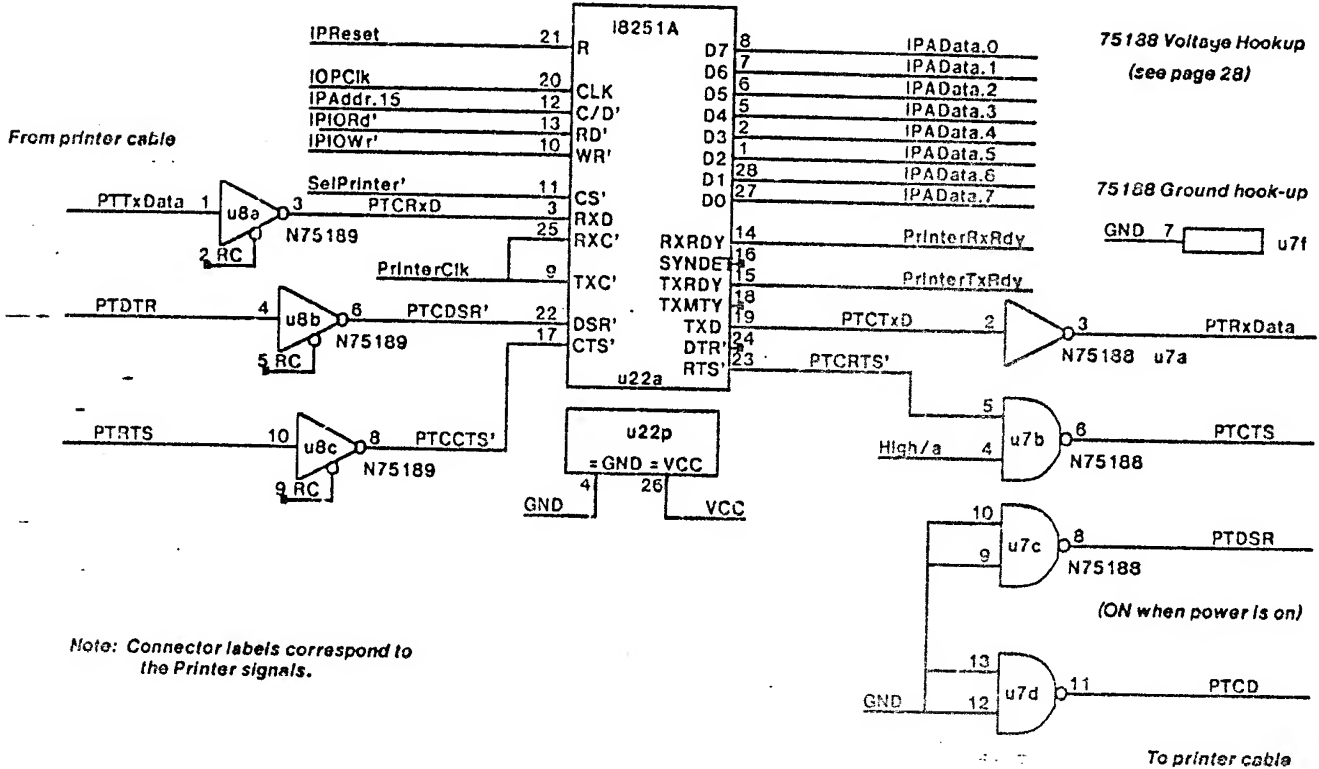
Currently, all devices on IPADData cause a Wait cycle.



I/O Processor Miscellaneous CPU control

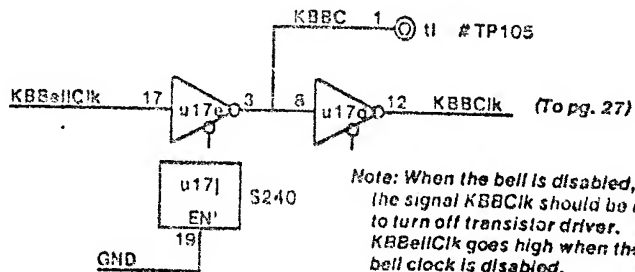
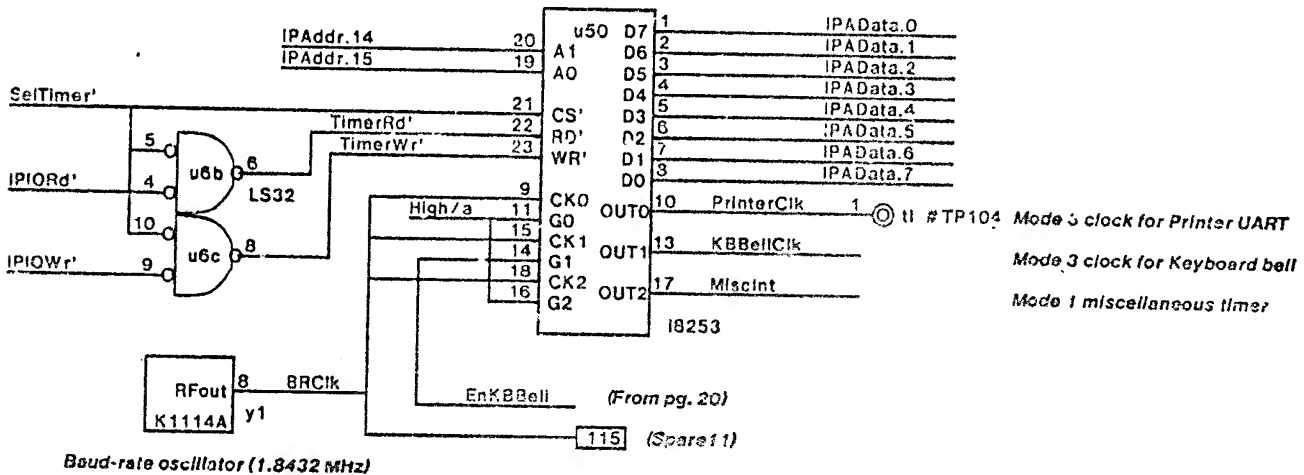
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 21 OF		

Printer UART



Note: Due to a design shortcoming the RD' and WR' lines of the 8253-5 must be externally qualified.

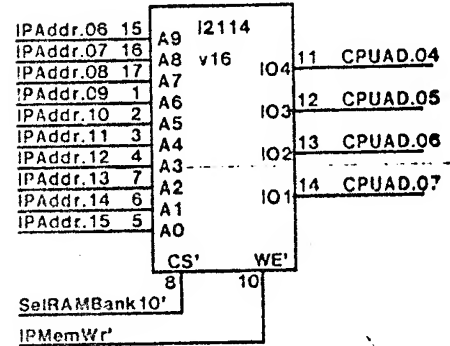
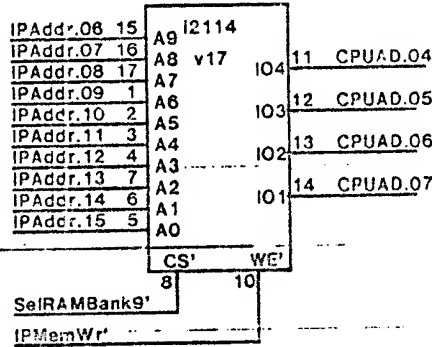
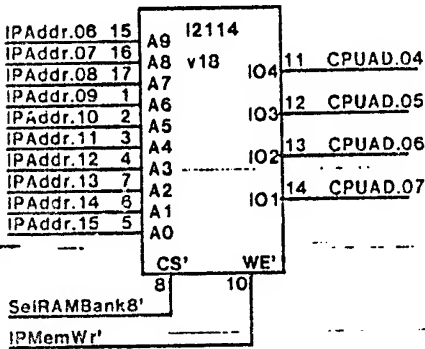
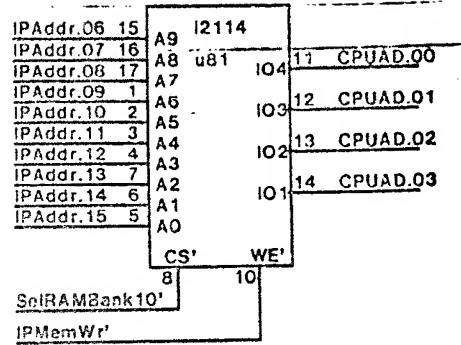
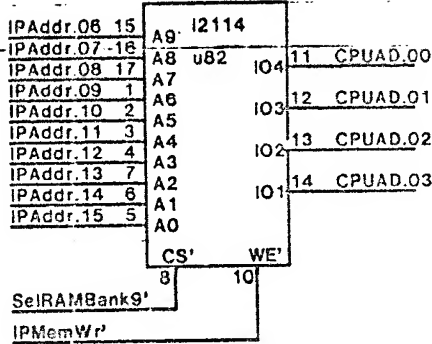
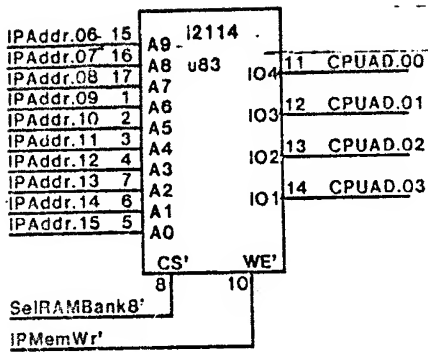
Baud-rate generator



I/O Processor Diablo Printer Interface

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 22 OF	

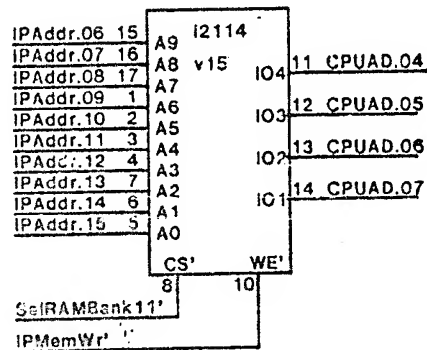
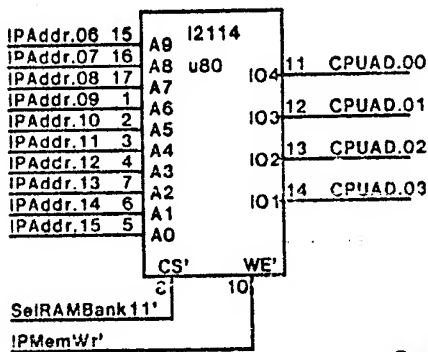
RAM - Banks 8 - 11



Bank 8

Bank 9

Bank 10

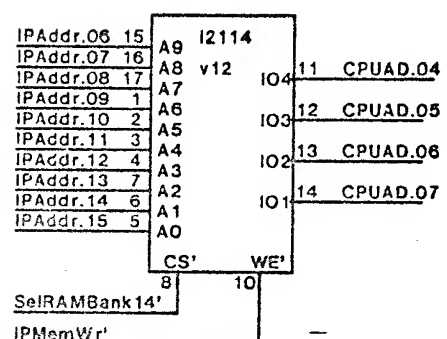
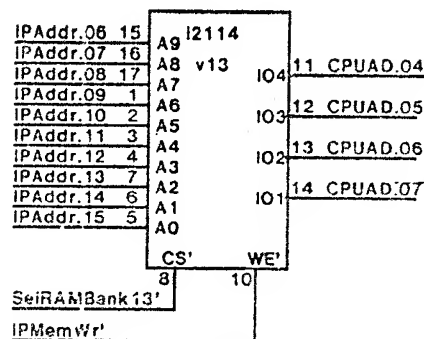
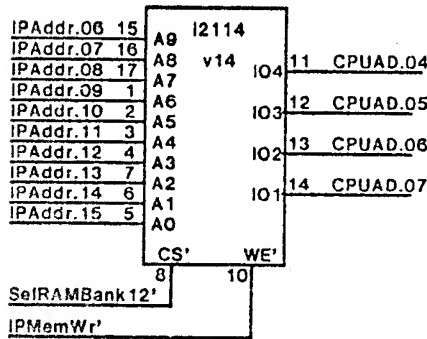
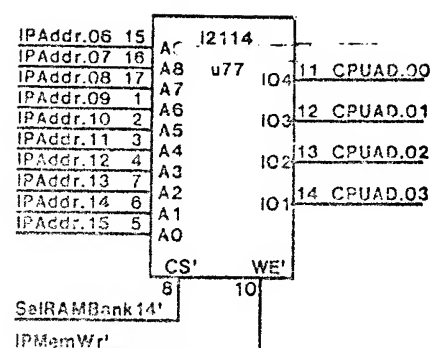
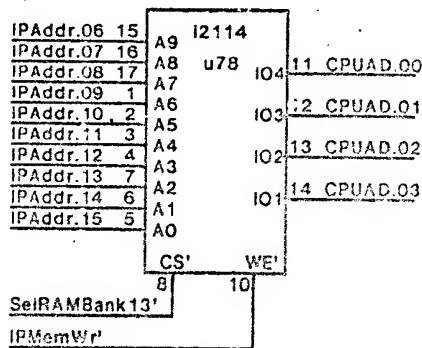
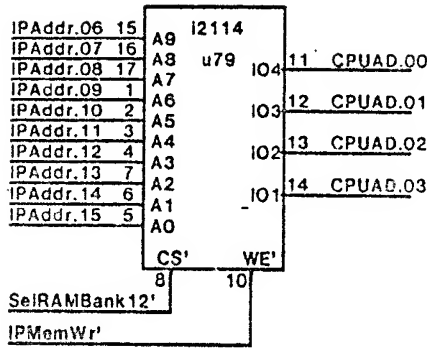


Bank 11

I/O Processor 4K RAM Memory-Banks 8-11

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 23 OF		

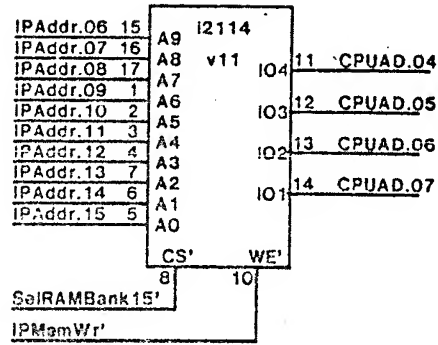
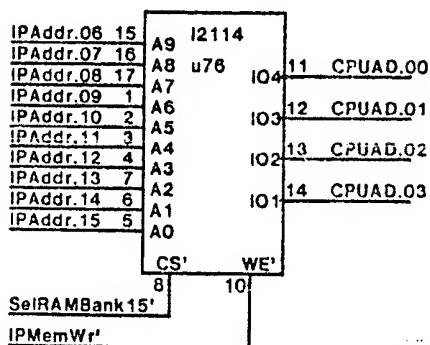
RAM - Banks 12 - 15



Bank 12

Bank 13

Bank 14



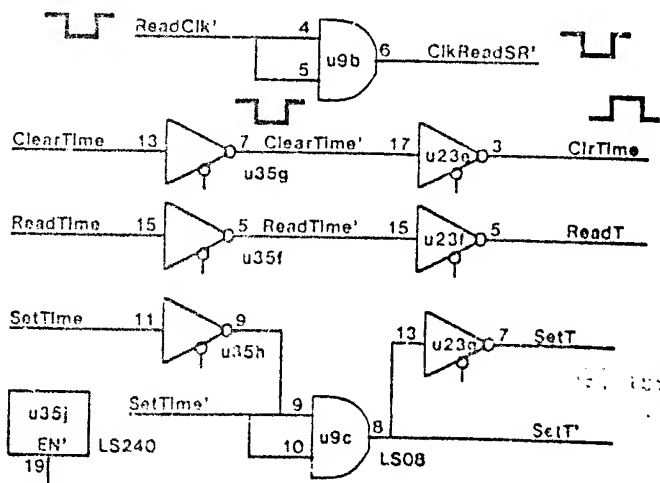
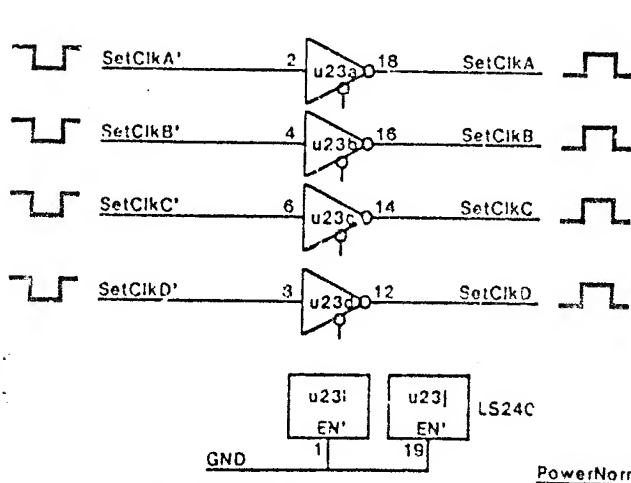
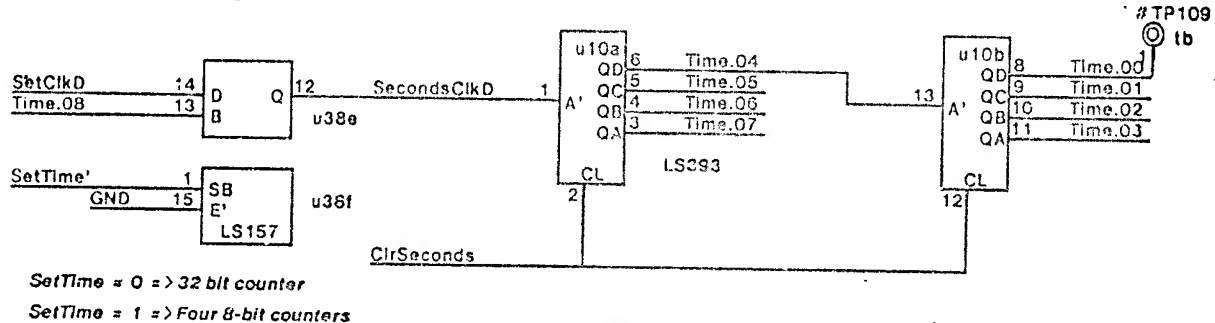
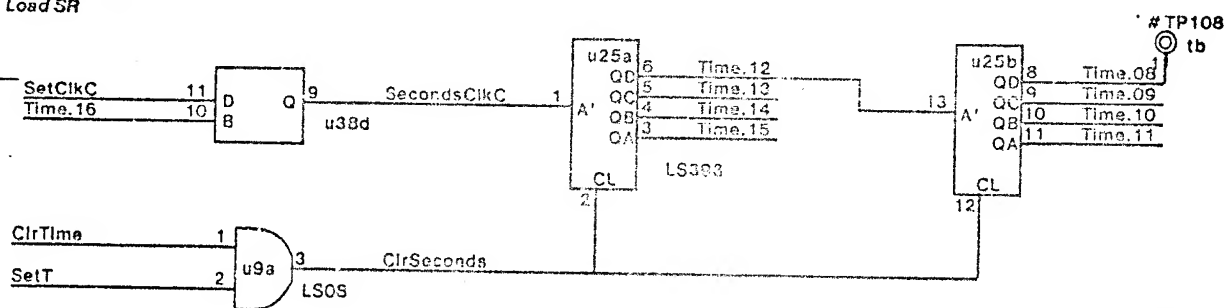
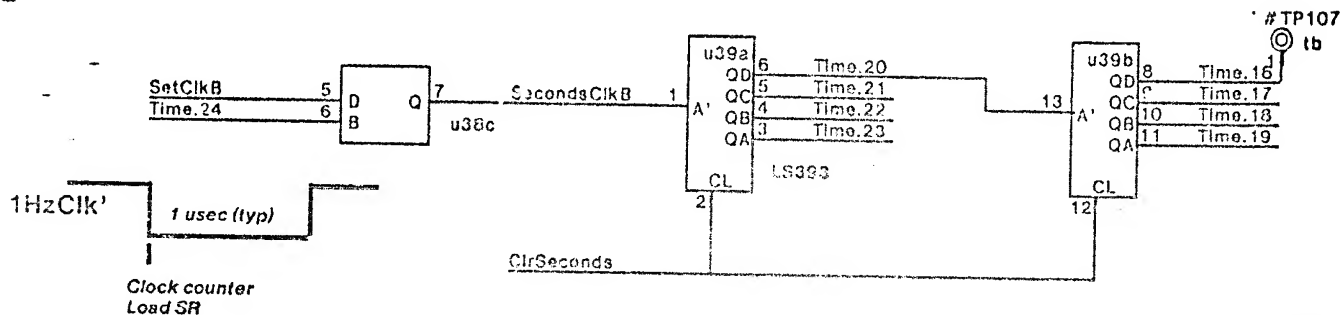
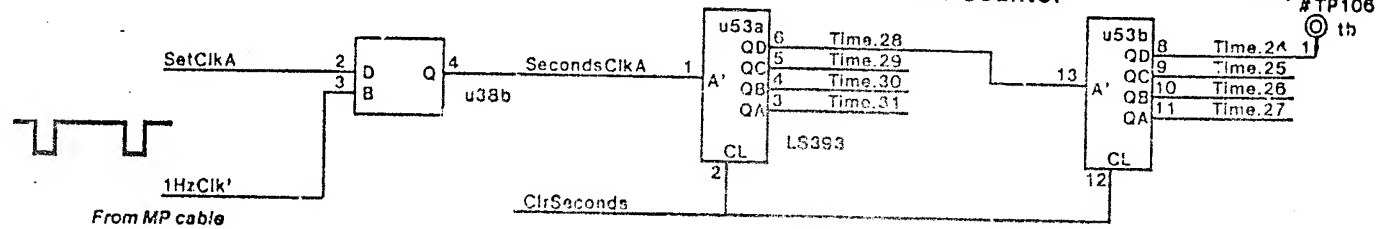
Bank 15

I/O Processor 4K RAM Memory-Banks 12-15

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 24 OF		

Note: All the logic on this page is powered from the Maintenance panel +5V supply, MV_{cc} (see page 26)

Seconds Counter



The 8 inputs SetClkA', SetClkB', SetClkC', SetClkD', ReadClk', ClearTime', ReadTime', SetTime' are pulled up for power-down condition.

I/O Processor Time-of-Day Clock - 1

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 25 OF		

Note: All the logic on this page is powered from the Maintenance panel +5V supply, MVCC

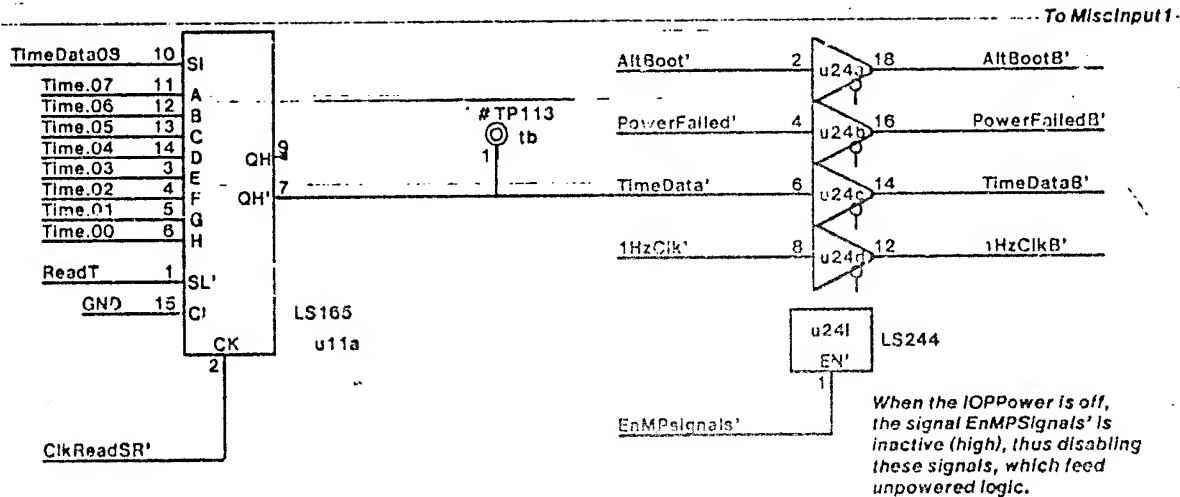
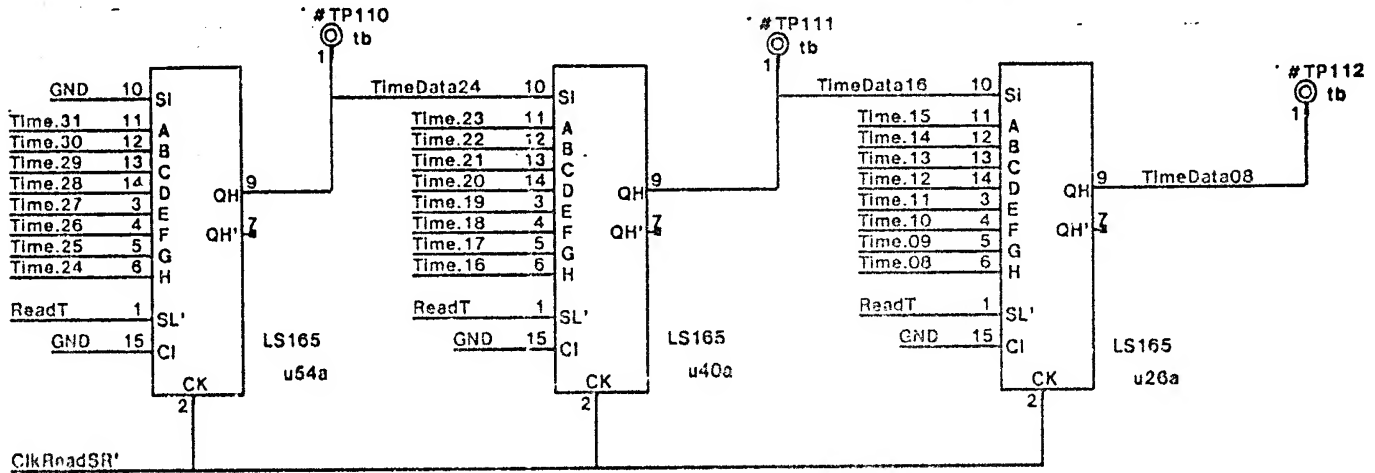
Time Read Shift Register

ReadTime = 0 =>

Shift register parallel loads Seconds Counter

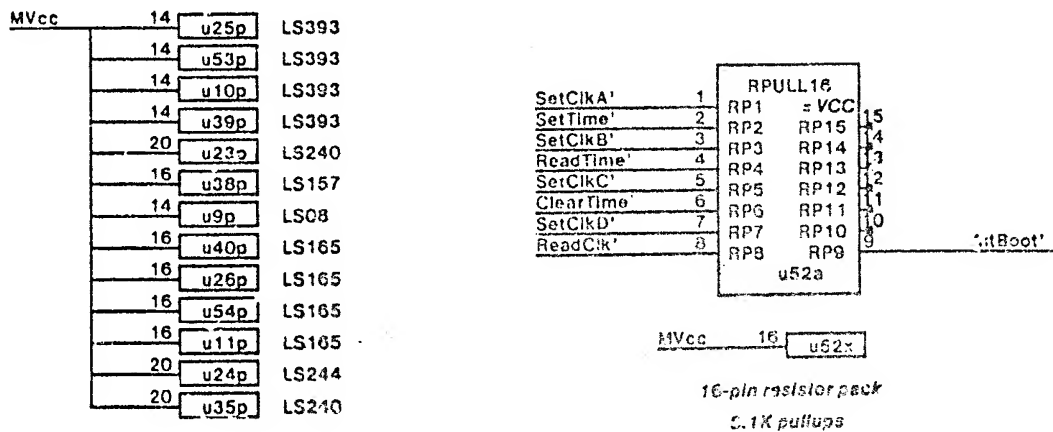
ReadTime = 1 =>

Shift register in serial shift mode, CkReadSR' clock



When the IOPower is off, the signal EnMPSignals' is inactive (high), thus disabling these signals, which feed unpowered logic.

Power for Time-of-day clock from Maintenance Panel

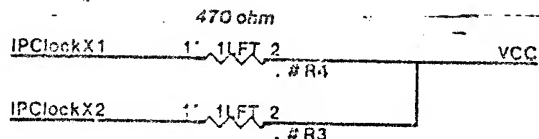
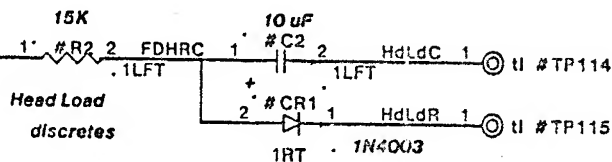
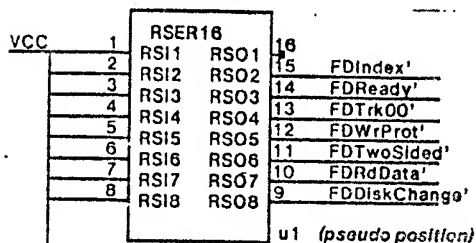


I/O Processor Time-of-Day Clock - 2

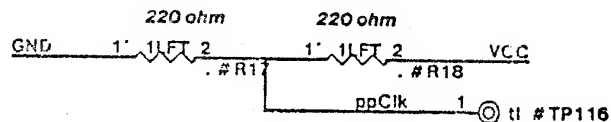
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE	DWG NO. 156P11952		SHEET REV.
	TITLE	SCHEMATIC. IOP	A4	SHEET 26 OF		

DISCRETE COMPONENTS (see also page 30)

Pullups, 150 ohm; 1/4 watt
Allen-Bradley 316B151

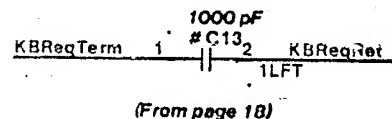
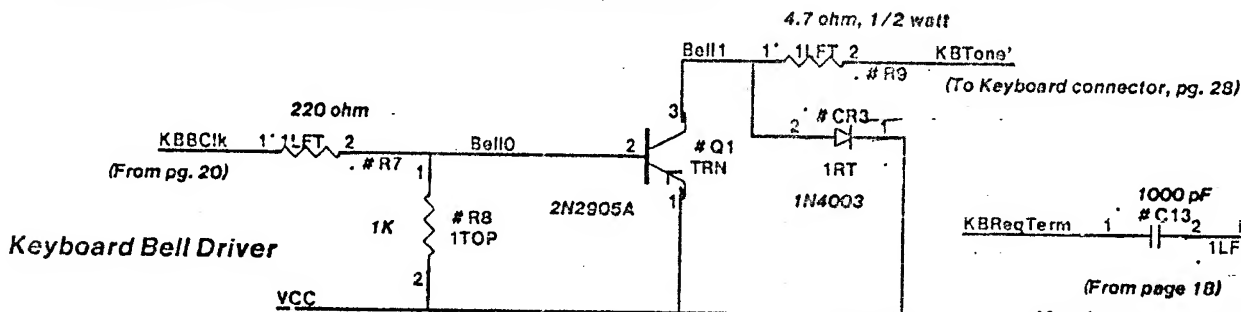


CPU clock driver pull-ups



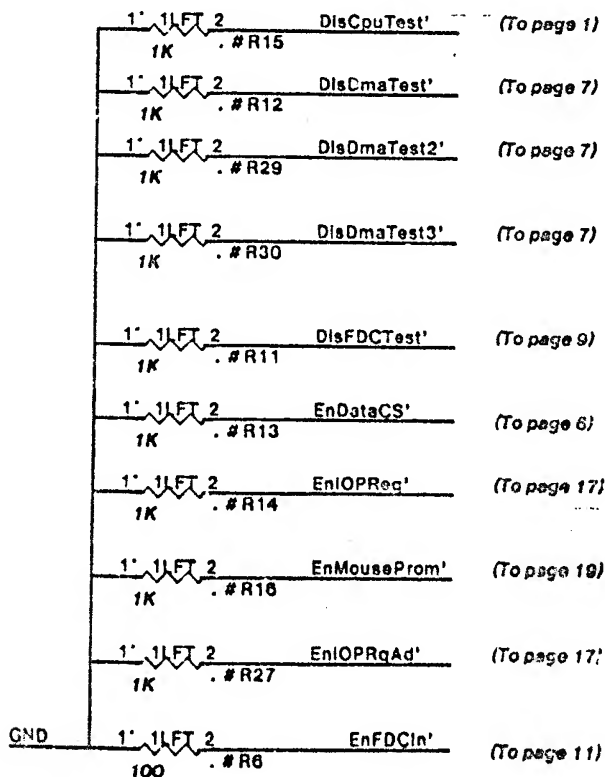
ppCik termination

Miscellaneous Floppy Controller discrete components



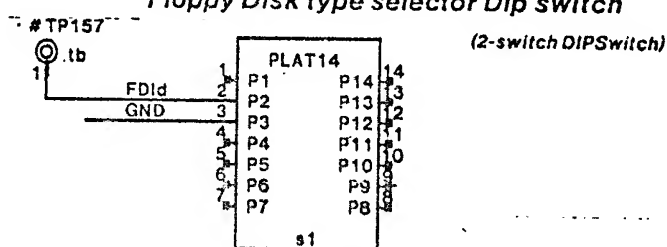
Keyboard Request Line

Discretes for Testability



Floppy Disk type selector Dip switch

(2-switch DIPSwitch)



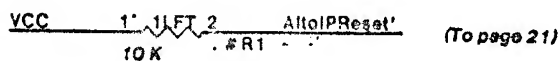
This is the switch to select the type of Floppy Disk drive in the system. Only 1 switch is needed, and should be the rightmost switch of a DIPSwitch package. The smallest package should be used. The package should be inserted in the spare position between u50 and u51, or below u74, whichever is easier, right adjusted. Shown here as position x51.

Examples: 4-switch DIP package: Grayhill 76RSB04 or 76SB04.

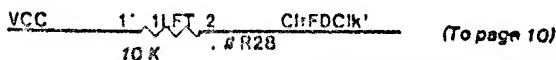
Xerox P/N 710W00004

2-switch DIP package: Grayhill 76RSB02 or 76SB02.

Pullups



(Needed for when no Alto is connected)



I/O Processor PC discretes

XEROX

PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS

TITLE SCHEMATIC, IOP

DWG SIZE A4

DWG NO. 156P11952

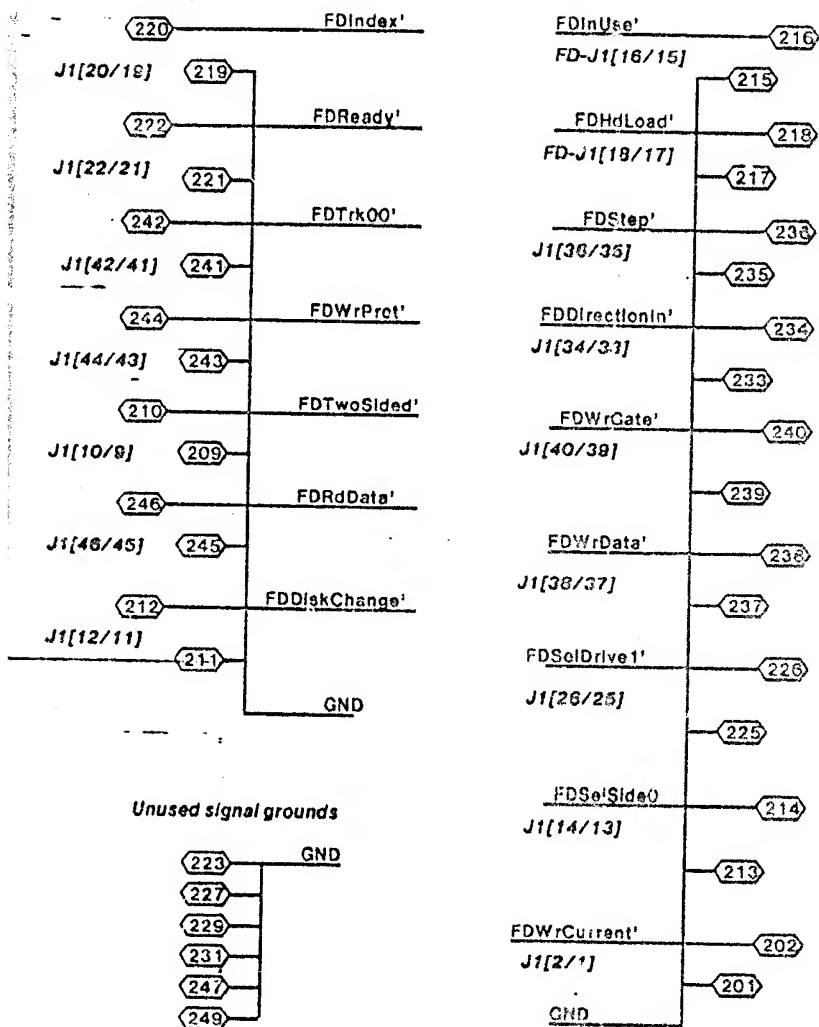
SHEET 27 OF

SHEET REV. B

Inputs

Outputs

(Printer)

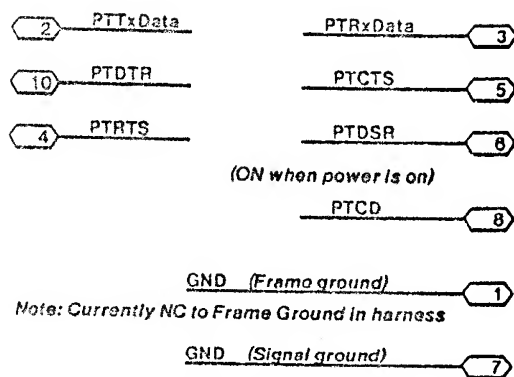


Floppy Disk Cable Connector

50-pin male connector

Xerox 713W14320

(Subtract 200 from above pin numbers to get physical pin number)



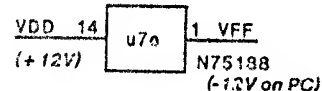
RS-232-C DCE port Cable Connector

10-pin male connector

Xerox 713W12220

(Above pin numbers are same as physical pin numbers)

75188 Voltage hookup

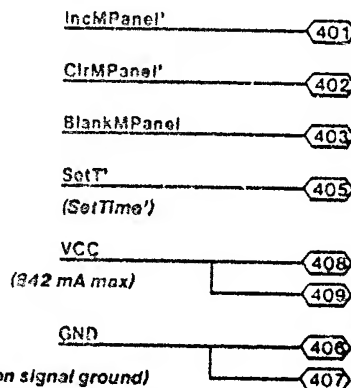
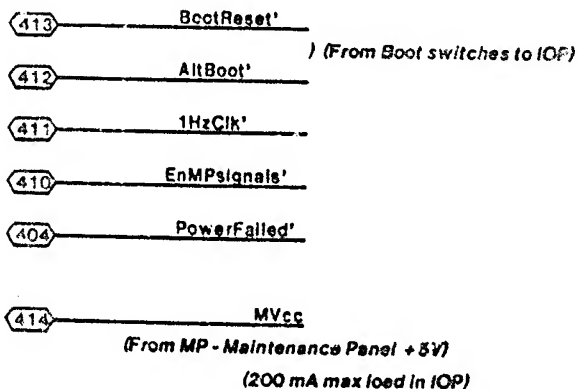


Maintenance Panel Cable Connector

14-pin male connector

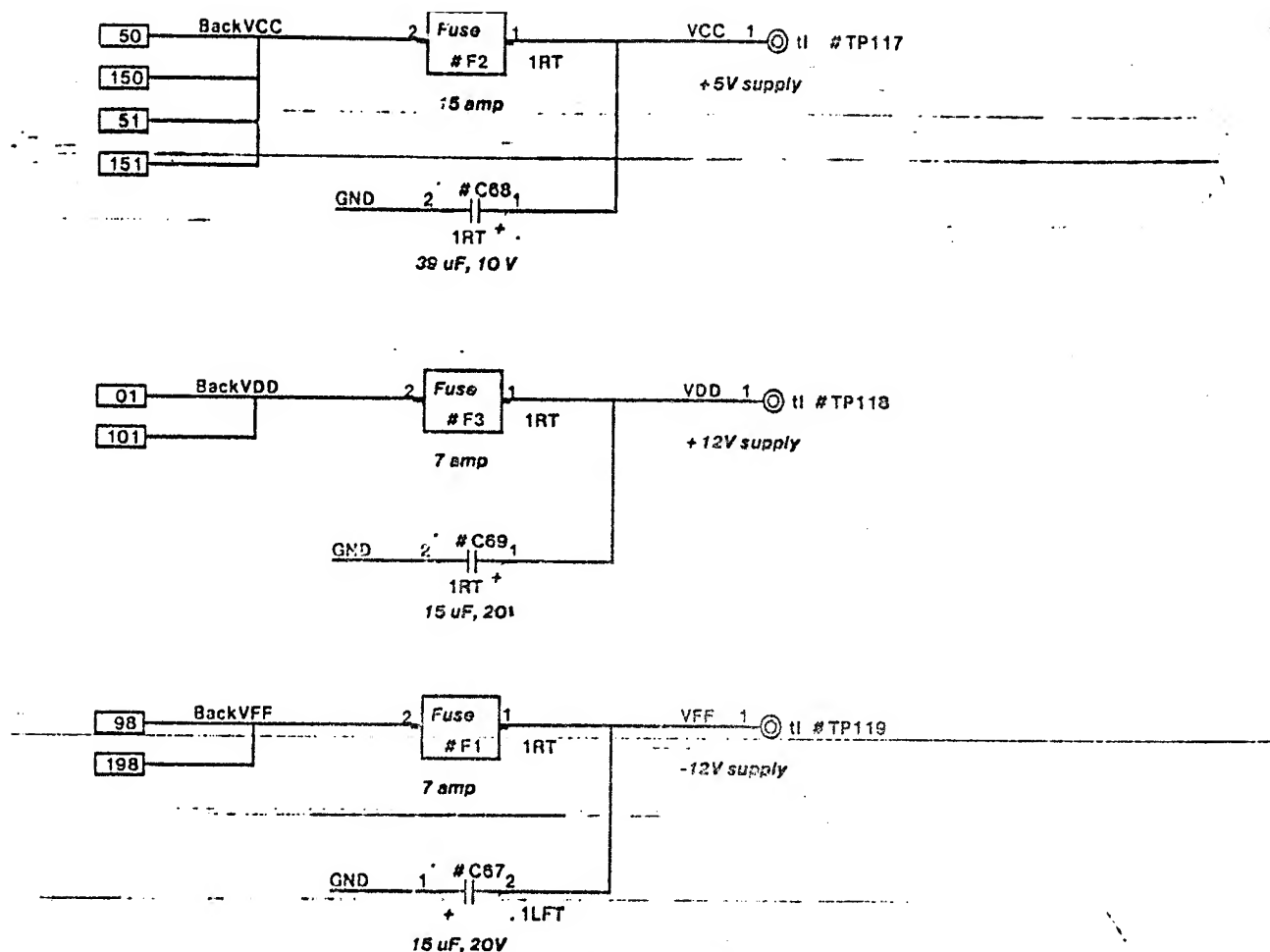
Xerox 713W13320

(Subtract 400 from pin numbers to get physical pin number)

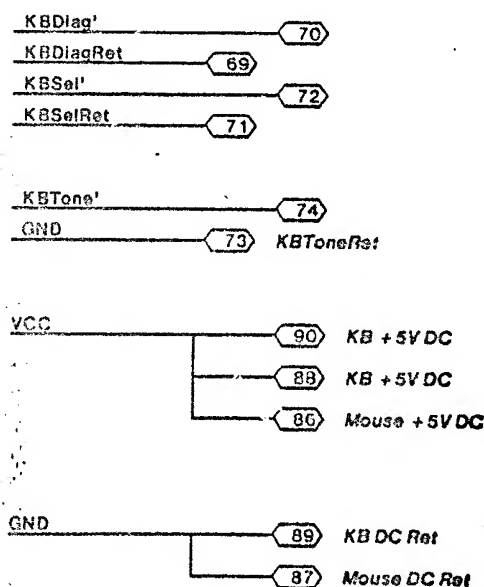
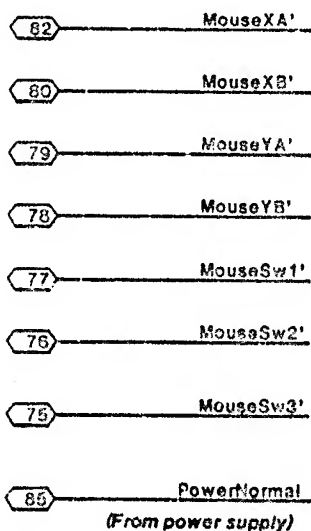
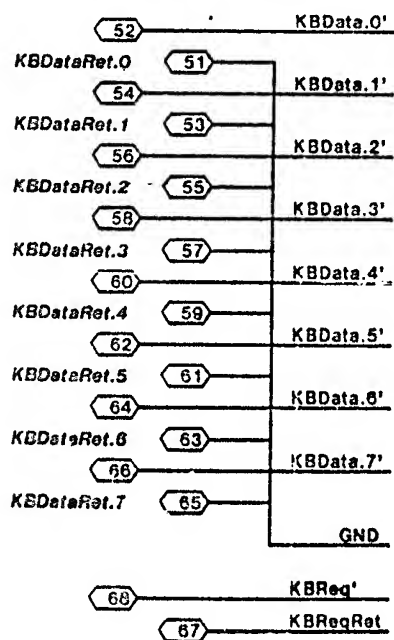


I/O Processor I/O Connectors - 2

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 28 OF		



CABLES



Keyboard cable connector

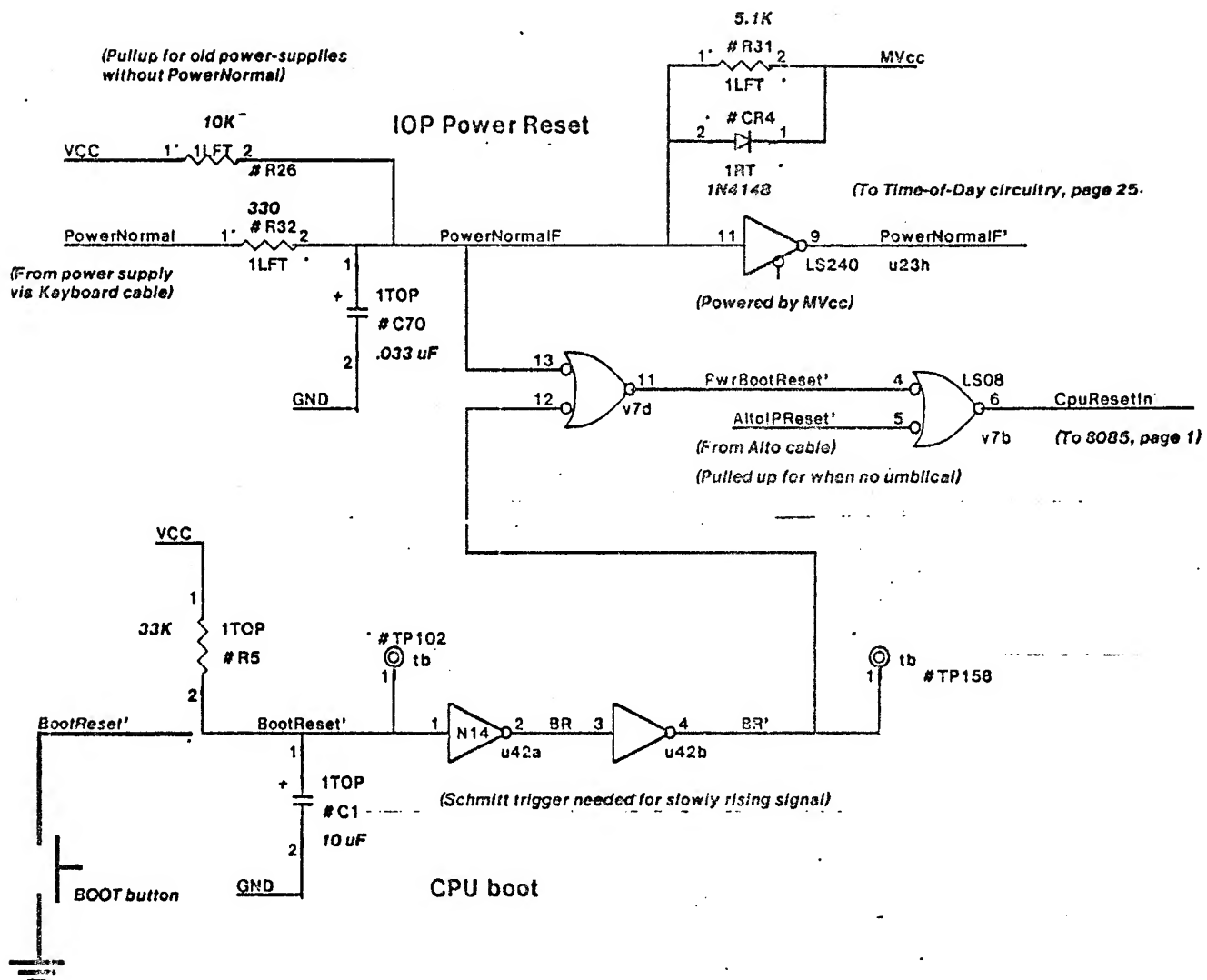
40-pin male connector

Xerox 713W12720

(Subtract 50 from above pin numbers to get physical pin number)

Power Supply and Fuses Keyboard cable connector

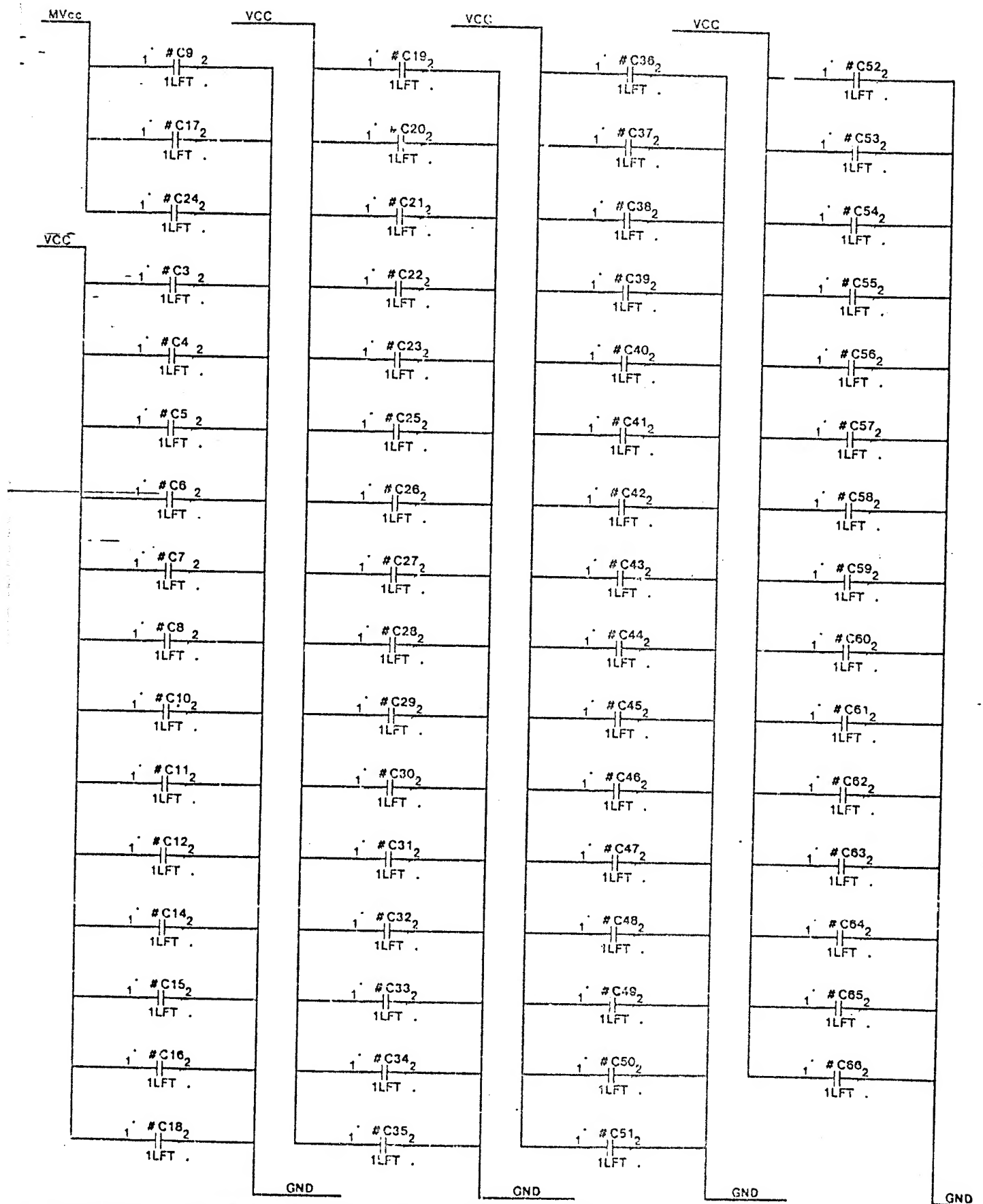
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 29 OF		



The PowerNormal signal is produced in new power supplies. This signal monitors the +5 V power. When +5 V initially rises after power-up, PowerNormal is low for 50 msec after the +5 V power has stabilized. On power down, PowerNormal is rapidly made low to cause an IOPReset before the power disappears.

I/O Processor: IOP Boot and Reset circuitry -

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP		A4	SHEET 30	OF	



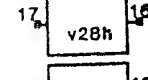
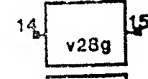
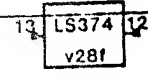
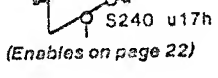
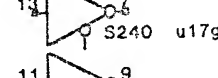
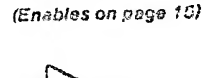
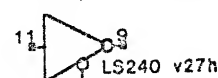
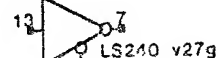
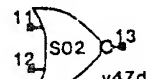
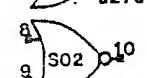
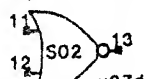
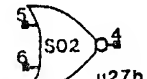
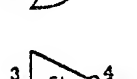
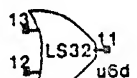
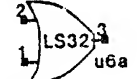
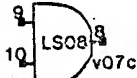
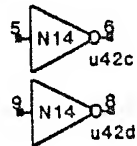
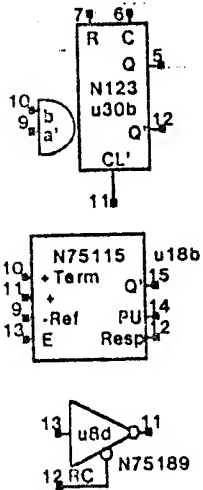
NOTE: All capacitors on this page are ceramic capacitors, 50V, 0.10 uf, part number 702W05218

DISCRETE CAPACITORS

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11952		SHEET REV. B
	TITLE SCHEMATIC, IOP			SHEET 31	OF	

Spares

(Enable on page 21)

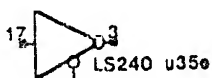
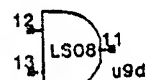


CPCIk

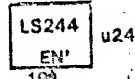
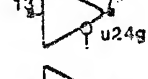
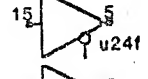
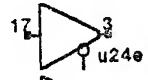
Also:

- LS244 (2), page 1
- LS244 (1), page 7
- LS244 (2), page 7
- LS244 (1), page 9
- LS153 (1), page 9
- LS157 (3), page 17

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(See page 25)



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I/O Processor Spares

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Comments:

- 1) Designator notation notes: u1-99 = U1-99, v0-99 = U100-199, w0-99 = U200-299
- 2) The last item on lines below, preceded by a semicolon (;), is the schematic page number on which the test point, connector or signal information originates.
- 3) Line with no page number was a continuation of the previous line.

#TP048	.1i	DisDmaTest'	:07	#TP145	.1i	CurState.1	:12
#TP1	.1i	AltoPPIIntA	:21	#TP146	.1i	CurState.2	:12
#TP10	.1i	CPUAD.07	:02	#TP147	.1i	CurState.3	:12
#TP100	.1i	UpMouseY	:19	#TP148	.1i	CurState.4	:12
#TP101	.1i	EnKBBell	:20	#TP149	.1i	CurState.5	:12
#TP102	.1i	BootReset'	:30	#TP15	.1i	CpuRD'	:01
#TP103	.1i	AltoIPReset'	:21	#TP150	.1i	CurState.6	:12
#TP104	.1i	PrinterClk	:22	#TP151	.1i	CPInWakeReqS	:17
#TP105	.1i	KBBC	:22	#TP152	.1i	CPOutWakeReqS	:17
#TP106	.1i	Time.24	:25	#TP153	.1i	IOPAttnSync'	:17
#TP107	.1i	Time.16	:25	#TP154	.1i	EnIOPRqAd'	:17
#TP108	.1i	Time.08	:25	#TP155	.1i	IPReady	:21
#TP109	.1i	Time.00	:25	#TP156	.1i	CpuReady	:21
#TP110	.1i	TimeData24	:26	#TP157	.1i	FDId	:27
#TP111	.1i	TimeData16	:26	#TP158	.1i	BR'	:30
#TP112	.1i	TimeData08	:26	#TP159	.1i	FloppyIntReq	:14
#TP113	.1i	TimeData'	:26	#TP16	.1i	CpuWR'	:01
#TP114	.1i	HdLdC	:27	#TP160	.1i	Int.5	:14
#TP115	.1i	HdLdR	:27	#TP162	.1i	CpuRST5	:14
#TP116	.1i	ppClk	:27	#TP163	.1i	DisDmaTest2'	:07
#TP117	.1i	VCC	:29	#TP164	.1i	DisDmaTest3'	:07
#TP118	.1i	VDD	:29	#TP17	.1i	CPUAddr.00	:01
#TP119	.1i	VFF	:29	#TP18	.1i	CPUAddr.01	:01
#TP12	.1i	IPReset	:01	#TP19	.1i	CPUAddr.02	:01
#TP120	.1i	SelHostAd'	:05	#TP2	.1i	CPAttn	:15
#TP121	.1i	SelPROMBank0'	:05	#TP20	.1i	CPUAddr.03	:01
#TP122	.1i	SelPROMBank1'	:05	#TP21	.1i	CPUAddr.04	:01
#TP123	.1i	SelPROMBank2'	:05	#TP22	.1i	CPUAddr.05	:01
#TP124	.1i	SelPROMBank3'	:05	#TP23	.1i	CPUAddr.06	:01
#TP125	.1i	SelRAMBank0'	:05	#TP24	.1i	CPUAddr.07	:01
#TP126	.1i	SelRAMBank1'	:05	#TP26	.1i	CpuHold	:01
#TP127	.1i	SelRAMBank2'	:05	#TP27	.1i	DisCpuTest'	:01
#TP128	.1i	SelRAMBank3'	:05	#TP28	.1i	PUI	:01
#TP129	.1i	SelRAMBank4'	:05	#TP29	.1i	SelAltoPPI'	:05
#TP13	.1i	CpuHoldAck	:01	#TP3	.1i	CPUAD.00	:02
#TP130	.1i	SelRAMBank5'	:05	#TP30	.1i	SelPrinter'	:05
#TP131	.1i	SelRAMBank6'	:05	#TP31	.1i	SelTimer'	:05
#TP132	.1i	SelRAMBank7'	:05	#TP32	.1i	ReadKBData'	:05
#TP133	.1i	SelRAMBank8'	:05	#TP33	.1i	ClrMouseXY'	:05
#TP134	.1i	SelRAMBank9'	:05	#TP34	.1i	IPADData.0	:06
#TP135	.1i	SelRAMBank10'	:05	#TP35	.1i	IPADData.1	:06
#TP136	.1i	SelRAMBank11'	:05	#TP36	.1i	IPADData.2	:06
#TP137	.1i	SelRAMBank12'	:05	#TP37	.1i	IPADData.3	:06
#TP138	.1i	SelRAMBank13'	:05	#TP38	.1i	IPADData.4	:06
#TP139	.1i	SelRAMBank14'	:05	#TP39	.1i	IPADData.5	:06
#TP14	.1i	CpuIO/M'	:01	#TP4	.1i	CPUAD.01	:02
#TP140	.1i	SelRAMBank15'	:05	#TP40	.1i	IPADData.6	:06
#TP141	.1i	DmaWaitReq	:06	#TP41	.1i	IPADData.7	:06
#TP142	.1i	ClrFDC1k'	:10	#TP42	.1i	EnIPData	:06
#TP143	.1i	FDCDbIDen'	:12	#TP43	.1i	EnIPADData'	:06
#TP144	.1i	FDCRC1k	:12	#TP44	.1i	EnIPADData	:06

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